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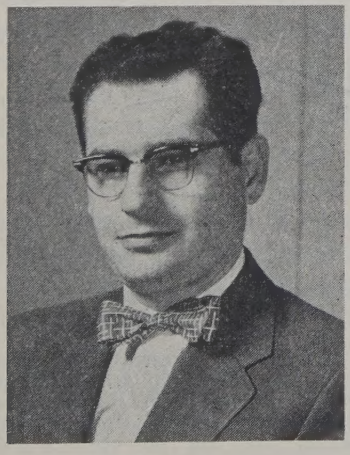

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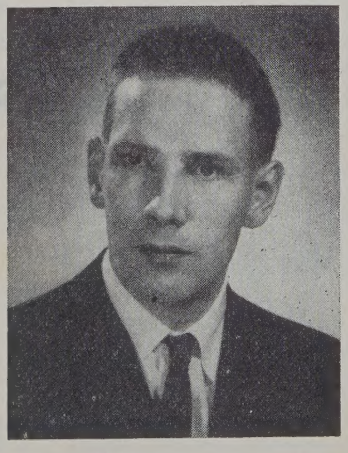

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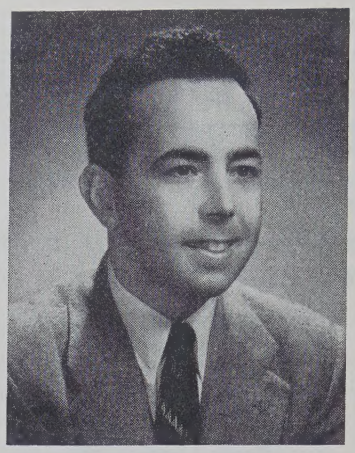

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"An Electronic Analog Computing Technique for the Solution of Trigonometric Problems"

IRE TRANSACTIONS ON ELECTRONIC COMPUTERS
Vol. EC-4, pp. 95–100; September, 1955

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A One-Microsecond Adder Using One-Megacycle Circuitry*

A. WEINBERGER† AND J. L. SMITH†

Summary—**An analysis of the functional representation of the carry digits in the addition process shows that the one-megacycle circuitry of SEAC and DYSEAC can be organized logically to permit the formation of many successive carries simultaneously. The Boolean expression for any carry digit C_k can be expanded so as to be an explicit function of only the input digits of orders k to $k-p+1$ and of the carry digit C_{k-p}. Certain factorizations can then be made to simplify these expressions so that all of them fall within the limitations on the gating complexity imposed by the circuitry.**

A parallel adder utilizing this principle is developed which is capable of adding two 53-bit numbers in one microsecond, with relatively few additional components over those required in a parallel adder of more conventional design.

Introduction

IN THE PAST, over-all computing speed has generally been limited by the rate at which memory references can be made, and for this reason a design principle adopted by the National Bureau of Standards has been to match the speed of the arithmetic unit to the speed of the memory chosen for a system. Accordingly, the earliest computer design at the National Bureau of Standards; *i.e.*, SEAC,[1] employed serial arithmetic circuits whose speed matched that of the fastest reliable memory available at that time, namely, the mercury acoustic-delay-line memory.

The subsequent development of faster memories, such as the Williams electrostatic, the magnetic-core, and more recently, the diode-capacitor[2,3] memories, made practical the design of faster arithmetic units to meet more stringent problem-solving requirements. To maintain an efficient speed match with the diode-capacitor memory, which can operate at speeds of the order of one random access per μsec, an arithmetic unit is required in which the average speed of processing words for the most common operations is of the order of one word per μsec. The problem then comes down to one of speeding up the basic addition rate, since addition is the most common operation and is the basis for the other arithmetic operations, such as subtraction, multiplication, and division, as well as for comparisons.

An attempt was made to speed up the arithmetic unit through logical organization alone, utilizing the basic one-mc circuitry which has proved successful in SEAC[1] and DYSEAC.[4,5] A study of the addition process led to the logical design of a parallel adder which is capable of adding two 53-bit numbers in one μsec with relatively few additional gating stages over the number required for a parallel adder of more conventional design.

Before discussing the adder in detail, a brief description of the logical capabilities of the SEAC circuitry[6] is in order. As shown in Fig. 1 the basic electronic unit consists essentially of three levels of diode gates in an OR-AND-OR logical array followed by a transformer-coupled pulse amplifier. The rate at which successive pulses pass through such a stage is determined by the clock frequency which is, in this case, 1 mc per second.

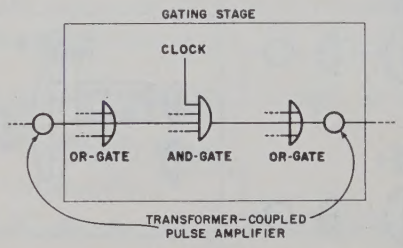

Fig. 1—One stage of SEAC-type circuitry.

The transit time of a pulse through a stage, however, is much less than one μsec. For this reason, the clock pulses are made available in several phases and different stages may be controlled by clock pulses of different phases as illustrated in Fig. 2. In SEAC, for example, one-

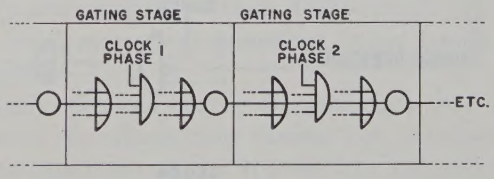

Fig. 2—SEAC stages clocked at different clock phases.

* Manuscript received by the PGEC, December 2, 1955.

† National Bureau of Standards, Washington, D.C.

[1] S. Greenwald, R. C. Haeuter, and S. N. Alexander, "SEAC," PROC. IRE, vol. 41, pp. 1300–1313; October, 1953. Also published in *National Bureau of Standards Circular 551*, pp. 5–26; January, 1955.

[2] A. W. Holt, "An experimental rapid access memory using diodes and capacitors," *Proc. ACM*, Toronto Meeting, pp. 132–142; December, 1952.

[3] R. J. Slutz, A. W. Holt, R. P. Witt, and D. C. Friedman, "High-speed memory developments at the National Bureau of Standards," *National Bureau of Standards Circular 551*, pp. 93–108; January, 1955.

[4] A. L. Leiner and S. N. Alexander, "System organization of the DYSEAC," TRANS. IRE, vol. EC-3, no. 1, pp. 1–10; March, 1954.

[5] A. L. Leiner, W. A. Notz, J. L. Smith, and A. Weinberger, "System design of the SEAC and DYSEAC," TRANS. IRE, vol. EC-3, no. 2, pp. 8–23; June, 1954.

[6] R. D. Elbourn, and R. P. Witt, "Dynamic circuit techniques used in SEAC and DYSEAC," PROC. IRE, vol. 41, pp. 1380–1387; October, 1953. Also published in TRANS. IRE, vol. EC-2, no. 1, pp. 2–9; March, 1953, and in *National Bureau of Standards Circular 551*, pp. 27–38; January, 1955.

mc pulses are available in 3 phrases, $\frac{1}{3}$ μsec apart. In DYSEAC, 4-phase clock pulses are used, while in the adder to be described a 5-phase clock is used. Fig. 3 shows graphically these timing relationships for SEAC. Signals resulting from several stages clocked at different times must be synchronized by means of electrical delay lines before they are gated in a common stage as shown

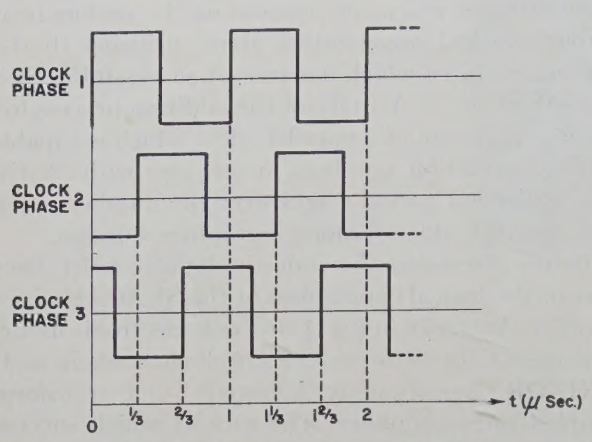

Fig. 3—Time relationships among SEAC clock pulses.

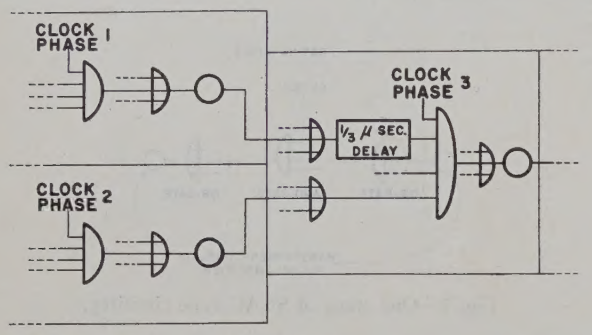

Fig. 4—Synchronization of SEAC pulses by means of delay lines.

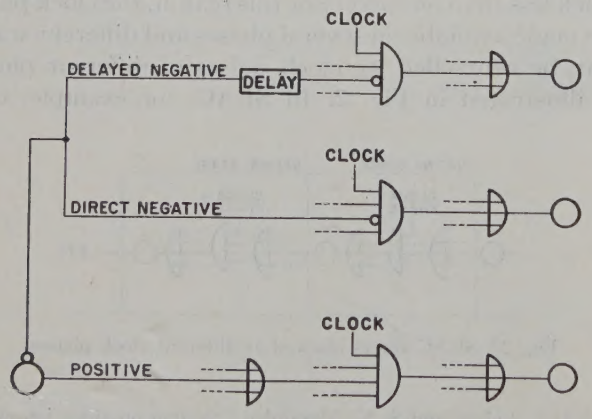

Fig. 5—Inhibiting by means of negative signals (direct or delayed).

in Fig. 4. Both positive and negative signals are available from a stage, the negative signals being used for inhibitions. See Fig. 5.

The maximum gating complexity used for a stage in the adder to be described is essentially the same as that employed in the packaged building blocks used in constructing DYSEAC, and therefore in the OR-AND-OR gating configuration of a stage up to 4 AND-gates and up to 6 inputs to an AND-gate are permissible.

Boolean notation of the sort described by Richards[7] will be used hereafter to describe the gating configurations. In Fig. 6 is shown a typical gating stage and the corresponding Boolean expression for the output in terms of the inputs. There are three terms in the expression, each one corresponding to an AND-gate; the first term, $(A+B)\overline{C}\,\overline{D}EF$, corresponds to the top AND-gate, the second term, $(G+H)I$ corresponds to the middle AND-gate, and the last term, $J(K+L+M)\overline{N}$, corresponds to the bottom AND-gate. The factors of a term represent the inputs to the corresponding AND-gate. For example, the five factors of the first term, $(A+B)$, $\overline{C}$, $\overline{D}$, E, and F correspond to the five inputs to the top AND-gate. Whenever a factor consists of more

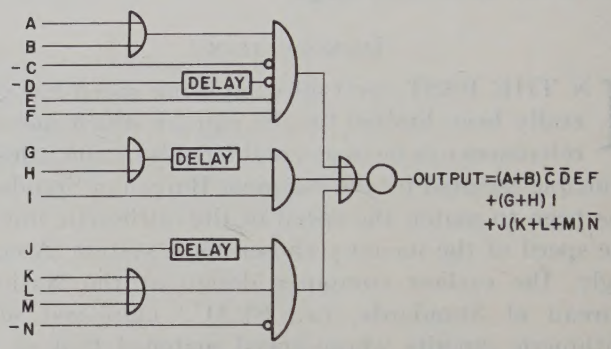

Fig. 6—Typical gating stage and corresponding Boolean expression.

than one term, it is represented by an OR-gate. For example, the factor $(A+B)$ of the first term corresponds to the 2-input OR-gate of the top AND-gate. A factor could also be a negative or inhibit signal and in this case it is denoted by a bar on top; *e.g.*, $\overline{C}$ and $\overline{D}$ are two factors of the first term corresponding to the two negative signals which may inhibit the top AND-gate. For the sake of simplicity in the Boolean expressions which follow, no distinction is made between delayed and undelayed signals.

Sequential Carry Generation

The analysis leading to the design of the parallel adder will now be described in detail.

Let

$$A = \text{augend} = A_k 2^{k-1} + A_{k-1}2^{k-2} + \cdots + A_1 2^0,$$
$$B = \text{addend} = B_k 2^{k-1} + B_{k-1}2^{k-2} + \cdots + B_1 2^0,$$
$$S = \text{sum} \quad = S_k 2^{k-1} + S_{k-1}2^{k-2} + \cdots + S_1 2^0,$$

and C_k = the carry resulting from the addition in the k-th digit position.

The well-known rules for binary addition are given in the form of a function table (Table I).

[7] R. K. Richards, "Arithmetic Operations in Digital Computers," D. Van Nostrand Company, Inc., New York, pp. 26–50; 1955.

TABLE I
FUNCTION TABLE FOR BINARY ADDITION

Augend	A_k	0	0	0	0	1	1	1	1
Addend	B_k	0	0	1	1	0	0	1	1
Previous Carry	C_{k-1}	0	1	0	1	0	1	0	1
Sum	S_k	0	1	1	0	1	0	0	1
Carry	C_k	0	0	0	1	0	1	1	1

From these, the binary sum and carry can be expressed in Boolean notation as

$$S_k = \overline{A}_k\overline{B}_kC_{k-1} + \overline{A}_kB_k\overline{C}_{k-1} + A_k\overline{B}_k\overline{C}_{k-1} + A_kB_kC_{k-1} \quad (1)$$

$$\left.\begin{aligned} C_k &= \overline{A}_kB_kC_{k-1} + A_k\overline{B}_kC_{k-1} + A_kB_k\overline{C}_{k-1} + A_kB_kC_{k-1} \\ &= A_kB_k + A_kC_{k-1} + B_kC_{k-1} \\ &= (A_k + B_k)(A_k + C_{k-1})(B_k + C_{k-1}) \\ &= A_kB_k + (A_k + B_k)C_{k-1} \end{aligned}\right\}. \quad (2)$$

The carry function, C_k, has been reduced from four terms of three factors each (corresponding to four AND-gates with three inputs each) as shown in the top line of (2) to three alternative forms each involving fewer terms and factors.

Since the expression for S_k in (1) can be implemented in one gating stage, any sum digit can be made available during the clock phase immediately following the formation of its corresponding carry, C_{k-1}. However, if the carries are generated according to (2), each carry digit would have to await the formation of the next lower-order carry. As a result, the sum digits would be obtained at the rate of one per clock phase, for if C_1 is available during the first clock phase, C_2 would be available during the second clock phase, C_3 during the third clock phase, etc. For numbers having n binary digits, $n-1$ possible carries would have to be provided for, requiring $n-1$ clock phases for their complete determination. If a four-phase, one-mc clock is used, four successive sum digits could be obtained during one μsec, Such an arrangement, using *sequential* carry generation would provide an increase of a factor of four in basic addition speed over the addition speed of a completely serial adder.

SIMULTANEOUS CARRY GENERATION

The limitation on the sequential method of forming the carries stems from the use of (2), which specifies C_k as an explicit function of C_{k-1}. It can be shown that C_k need not depend explicitly on C_{k-1}, but can be expressed as a function of only the relevant augend and addend digits and C_0. C_0 is equivalent to a carry which, together with the least significant augend and addend digits, forms the least significant sum digit, thus

$$S_1 = \overline{A}_1\overline{B}_1C_0 + A_1B_1\overline{C}_0 + A_1\overline{B}_1\overline{C}_0 + A_1B_1C_0. \quad (3)$$

C_0 is used during addition cycles requiring the adding of 1 to the sum, such as the adding of negative numbers in complementary form.

In order to keep the expanded algebraic expressions concise the following abbreviations in the notation are introduced.

$$\left.\begin{aligned} D_k &\equiv A_kB_k \\ R_k &\equiv (A_k + B_k) \end{aligned}\right\}. \quad (4)$$

The expression for C_k can now be expanded as

$$\left.\begin{aligned} C_k &= A_kB_k + (A_k + B_k)C_{k-1} \equiv D_k + R_kC_{k-1} \\ &= D_k + R_kD_{k-1} + R_kR_{k-1}C_{k-2} \\ &\vdots \\ &= D_k + R_kD_{k-1} + R_kR_{k-1}D_{k-2} + \cdots \\ &\quad + R_kR_{k-1}\cdots R_2R_1C_0 \end{aligned}\right\}. \quad (5)$$

For the highest-order carries, the expanded relation becomes too large to be performed logically in one gating stage. In fact, to form C_k as in the last expression of (5), $(k+1)$ AND-gates and an equal number of inputs to the largest AND-gate would normally be required.

Nevertheless, a considerable gain in speed may be obtained by expanding C_k until the maximum permissible gating complexity is reached. By this means, up to four successive carries may be formed simultaneously in one clock phase as shown in (6).

$$\left.\begin{aligned} C_k &= D_k + R_kD_{k-1} + R_kR_{k-1}D_{k-2} + R_kR_{k-1}R_{k-2}D_{k-3} \\ &\quad + R_kR_{k-1}R_{k-2}R_{k-3}C_{k-4} \\ &= D_k + R_kD_{k-1}D_{k-2} \\ &\quad + R_kR_{k-1}R_{k-2}R_{k-3}(A_{k-3} + C_{k-4})(B_{k-3} + C_{k-4}) \\ C_{k-1} &= D_{k-1} + R_{k-1}D_{k-2} + R_{k-1}R_{k-2}D_{k-3} \\ &\quad + R_{k-1}R_{k-2}R_{k-3}C_{k-4} \\ C_{k-2} &= D_{k-2} + R_{k-2}D_{k-3} + R_{k-2}R_{k-3}C_{k-4} \\ C_{k-3} &= D_{k-3} + R_{k-3}C_{k-4} \end{aligned}\right\}. \quad (6)$$

This expression for C_k ,which represents the most complicated gating structure of the four, is reduced to four terms (corresponding to four AND-gates), the largest having six factors (corresponding to six inputs to the AND-gate).

Similarly, the four carries C_{k-4} through C_{k-7} can also be formed simultaneously during the previous clock phase as functions of the appropriate augend and addend digits and C_{k-8}. In short, four successive carry digits can be formed simultaneously every clock phase. One gating stage per carry is required.

The expressions (6) indicate that if C_0 is available during the first clock phase, C_1 through C_4 can be made available during the second clock phase, C_5 through C_8 during the third clock phase, etc. Each group of sum digits can be obtained one clock phase after the appropriate group of carries has been formed. Fig. 7 illustrates in block-diagram form an adder utilizing this principle of simultaneous carry generation.

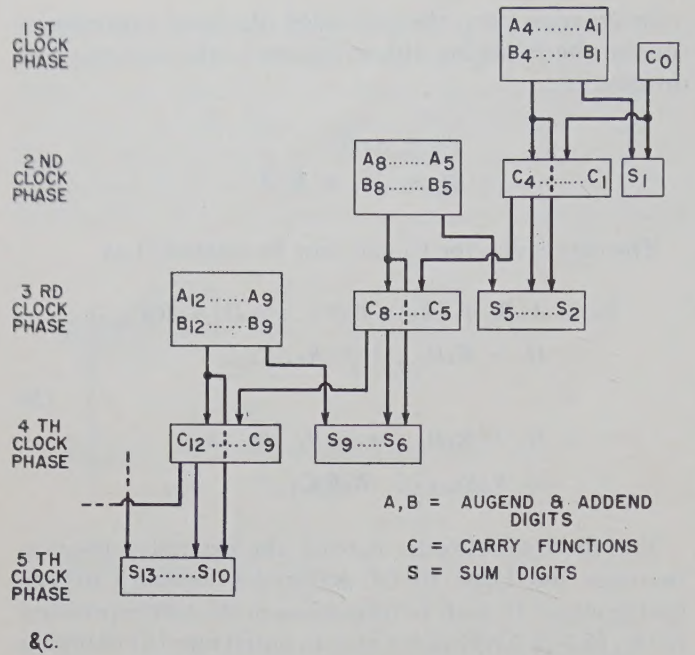

Fig. 7—Formation of parallel groups of sum digits.

Use of Auxiliary Carry Functions

Means for further increasing the addition speed by increasing the number of carries obtained during one clock phase will now be described. This method involves the use of some auxiliary functions defined in the following manner. The last expression in (5) is rewritten, expanded to the order $k-25$. See Table II. This equation is written in triangular form with one term per row in order to make the common factors more easily discernible. The auxiliary carry function X is defined as those parts of the terms shown in Table II lying within the small triangles along the hypotenuse of the large triangle, and the auxiliary carry function Y is defined as those parts of the terms lying within the rectangles. The subscript assigned to any X or Y is the one at the left of the corresponding triangle or rectangle.

Substituting X's and Y's into the expression for C_k in Table II with the appropriate subscripts, the following equation is obtained.

$$\left.\begin{aligned} C_k &= X_k + Y_k X_{k-5} + Y_k Y_{k-5} X_{k-10} + Y_k Y_{k-5} Y_{k-10} X_{k-15} \\ &\quad + Y_k Y_{k-5} Y_{k-10} Y_{k-15} X_{k-20} \\ &\quad + Y_k Y_{k-5} Y_{k-10} Y_{k-15} Y_{k-20} C_{k-25} \\ &= X_k + Y_k X_{k-5} \\ &\quad + Y_k Y_{k-5} (X_{k-10} + Y_{k-10})(X_{k-10} + X_{k-15}) \\ &\quad + Y_k Y_{k-5} Y_{k-10} Y_{k-15} (X_{k-20} + Y_{k-20}) \\ &\quad \cdot (X_{k-20} + C_{k-25}) \end{aligned}\right\}. \quad (7)$$

In order to form these functions X and Y, an extra clock phase must be provided between the input stages and the carry stages. Since the functions Y consist of only a single term of five factors, they can easily be

TABLE II

Expansion of C_k in Terms of Augend and Addend Digits and C_{k-25}
D_k Represents A_kB_k; R_k Represents (A_k+B_k)

$C_k =$

D_k
+ $R_k\ D_{k-1}$
+ $R_k\ R_{k-1}\ D_{k-2}$
+ $R_k\ R_{k-1}\ R_{k-2}\ D_{k-3}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ D_{k-4}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ D_{k-5}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ D_{k-6}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ D_{k-7}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ D_{k-8}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ D_{k-9}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ D_{k-10}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ D_{k-11}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ D_{k-12}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ D_{k-13}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ D_{k-14}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ D_{k-15}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ R_{k-15}\ D_{k-16}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ R_{k-15}\ R_{k-16}\ D_{k-17}$
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+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ R_{k-15}\ R_{k-16}\ R_{k-17}\ R_{k-18}\ R_{k-19}\ R_{k-20}\ D_{k-21}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ R_{k-15}\ R_{k-16}\ R_{k-17}\ R_{k-18}\ R_{k-19}\ R_{k-20}\ R_{k-21}\ D_{k-22}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ R_{k-15}\ R_{k-16}\ R_{k-17}\ R_{k-18}\ R_{k-19}\ R_{k-20}\ R_{k-21}\ R_{k-22}\ D_{k-23}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ R_{k-15}\ R_{k-16}\ R_{k-17}\ R_{k-18}\ R_{k-19}\ R_{k-20}\ R_{k-21}\ R_{k-22}\ R_{k-23}\ D_{k-24}$
+ $R_k\ R_{k-1}\ R_{k-2}\ R_{k-3}\ R_{k-4}\ R_{k-5}\ R_{k-6}\ R_{k-7}\ R_{k-8}\ R_{k-9}\ R_{k-10}\ R_{k-11}\ R_{k-12}\ R_{k-13}\ R_{k-14}\ R_{k-15}\ R_{k-16}\ R_{k-17}\ R_{k-18}\ R_{k-19}\ R_{k-20}\ R_{k-21}\ R_{k-22}\ R_{k-23}\ R_{k-24}\ C_{k-25}$

$C_k =$

X_k
+ $Y_k\ X_{k-5}$
+ $Y_k\ Y_{k-5}\ X_{k-10}$
+ $Y_k\ Y_{k-5}\ Y_{k-10}\ X_{k-15}$
+ $Y_k\ Y_{k-5}\ Y_{k-10}\ Y_{k-15}\ X_{k-20}$
+ $Y_k\ Y_{k-5}\ Y_{k-10}\ Y_{k-15}\ Y_{k-20}\ C_{k-25}$

implemented in single gating stages during the intermediate clock phase. The functions X as they appear in Table II consist of five terms, and hence appear too complicated to be implemented in single gating stages. However, the first two terms of each X, of the form $D_k+R_kD_{k-1}$, are easily reduced to one term, as follows,

$$\left.\begin{aligned} D_k + R_kD_{k-1} &= A_kB_k + (A_k + B_k)A_{k-1}B_{k-1} \\ &= (A_k + B_k)(A_k + A_{k-1})(A_k + B_{k-1}) \\ &\quad \cdot(B_k + A_{k-1})(B_k + B_{k-1}) \\ &\equiv F_k \end{aligned}\right\}, \quad (8)$$

so that each X can in fact be formed in a single gating stage during the intermediate clock phase. F_k is introduced as an abbreviation in the notation to denote the conjunctive form in (8) which can be implemented in one AND-gate. The explicit expressions for X and Y are given in Table III.

TABLE III

EXPRESSIONS FOR FIRST-LEVEL AUXILIARY CARRY FUNCTIONS

$$\begin{aligned}
X_k &= F_k+R_kR_{k-1}D_{k-2}+R_kR_{k-1}R_{k-2}D_{k-3}+R_kR_{k-1}R_{k-2}R_{k-3}D_{k-4} \\
Y_k &= R_kR_{k-1}R_{k-2}R_{k-3}R_{k-4} \\
X_{k-5} &= F_{k-5}+R_{k-5}R_{k-6}D_{k-7}+R_{k-5}R_{k-6}R_{k-7}D_{k-8} \\
&\quad +R_{k-5}R_{k-6}R_{k-7}R_{k-8}D_{k-9} \\
Y_{k-5} &= R_{k-5}R_{k-6}R_{k-7}R_{k-8}R_{k-9} \\
X_{k-10} &= F_{k-10}+R_{k-10}R_{k-11}D_{k-12}+R_{k-10}R_{k-11}R_{k-12}D_{k-13} \\
&\quad +R_{k-10}R_{k-11}R_{k-12}R_{k-13}D_{k-14} \\
Y_{k-10} &= R_{k-10}R_{k-11}R_{k-12}R_{k-13}R_{k-14} \\
X_{k-15} &= F_{k-15}+R_{k-15}R_{k-16}D_{k-17}+R_{k-15}R_{k-16}R_{k-17}D_{k-18} \\
&\quad +R_{k-15}R_{k-16}R_{k-17}R_{k-18}D_{k-19} \\
Y_{k-15} &= R_{k-15}R_{k-16}R_{k-17}R_{k-18}R_{k-19} \\
X_{k-20} &= F_{k-20}+R_{k-20}R_{k-21}D_{k-22}+R_{k-20}R_{k-21}R_{k-22}D_{k-23} \\
&\quad +R_{k-20}R_{k-21}R_{k-22}R_{k-23}D_{k-24} \\
Y_{k-20} &= R_{k-20}R_{k-21}R_{k-22}R_{k-23}R_{k-24}
\end{aligned}$$

F_k represents $(A_k+B_k)(A_k+A_{k-1})(A_k+B_{k-1})(B_k+A_{k-1})(B_k+B_{k-1})$
D_k represents A_kB_k
R_k represents (A_k+B_k)

The second expression in (7), containing the maximum allowable number of terms and factors per term, indicates that the expansion of C_k can be carried out to 25 orders without exceeding the limitations of gating complexity.

The other carries C_{k-1} through C_{k-24} can likewise be expressed as functions of appropriate auxiliary carry functions and of C_{k-25}, and therefore they can be formed simultaneously with C_k. For example, the expression for C_{k-1}, shown in (9), is a function of the *same elements* as is C_k, with the exception that X_{k-1} and Y_{k-1} are substituted for X_k and Y_k.

$$\left.\begin{aligned} C_{k-1} &= X_{k-1} + Y_{k-1}X_{k-5} \\ &\quad + Y_{k-1}Y_{k-5}(X_{k-10} + Y_{k-10})(X_{k-10} + X_{k-15}) \\ &\quad + Y_{k-1}Y_{k-5}Y_{k-10}Y_{k-15}(X_{k-20} + Y_{k-20}) \\ &\quad \cdot(X_{k-20} + C_{k-25}) \end{aligned}\right\}. \quad (9)$$

The expressions for X_{k-1} and Y_{k-1} are shown in (10).

$$\left.\begin{aligned} X_{k-1} &= D_{k-1} + R_{k-1}D_{k-2} + R_{k-1}R_{k-2}D_{k-3} \\ &\quad + R_{k-1}R_{k-2}R_{k-3}D_{k-4} \\ Y_{k-1} &= R_{k-1}R_{k-2}R_{k-3}R_{k-4} \end{aligned}\right\}. \quad (10)$$

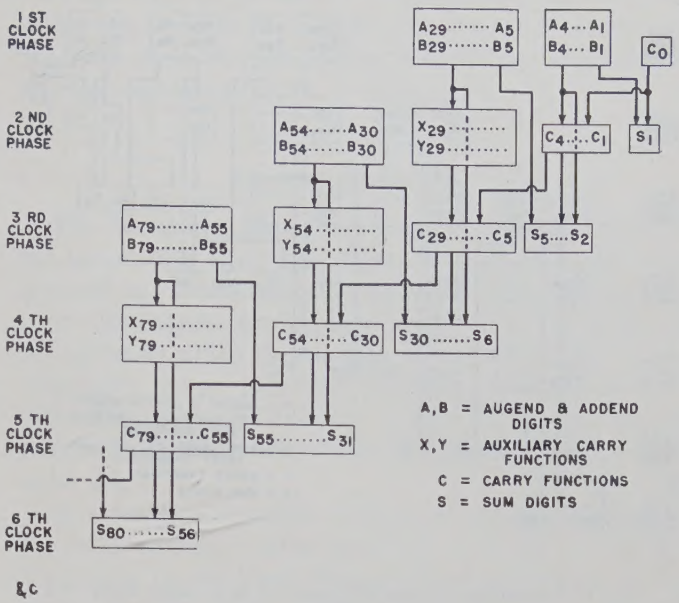

Fig. 8—Formation of parallel groups of sum digits using one level of auxiliary carry functions.

Similarly, other auxiliary carry functions need to be formed in order to obtain all 25 carries, C_k through C_{k-24}, simultaneously. The lower-order carries require progressively less complicated gating.

Fig. 8 illustrates in block-diagram form an adder employing these auxiliary carry functions. The four carries C_1 through C_4 are formed as in Fig. 7. Each succeeding group of 25 carries is formed during successive clock phases. Sum digits are, as usual, obtained by means of (1).

TWO-LEVEL AUXILIARY FUNCTIONS

A further increase in addition speed, through the ability to form more than 25 carries simultaneously in each clock phase, can be achieved if the method just described is extended to include two or more levels of auxiliary carry functions. The second level would consist of gating stages combining groups of first-level functions, the third level combining groups of second-level functions, etc. The final carry functions would combine groups of the last level of auxiliary carry functions. However, for each level of auxiliary carry functions between the input digits and the final carry digits, it is necessary to provide one extra clock phase.

Fig. 9 illustrates in block-diagram form an adder using two levels of auxiliary carry functions, the first level consisting of sets of X's and Y's and the second level consisting of sets of Z's and W's. The Z's and W's are formed from groups of X's and Y's and the final carry functions are formed from groups of Z's, W's, and the most significant of the carries formed during the previous clock phase.

In the illustration of Fig. 9, C_1 through C_{29} are formed as in the previous block diagram (Fig. 8). The next 150 carries, C_{30} through C_{179}, can be formed simultaneously one clock phase following C_{29}. Each succeeding clock phase, another group of 150 carries can be obtained.

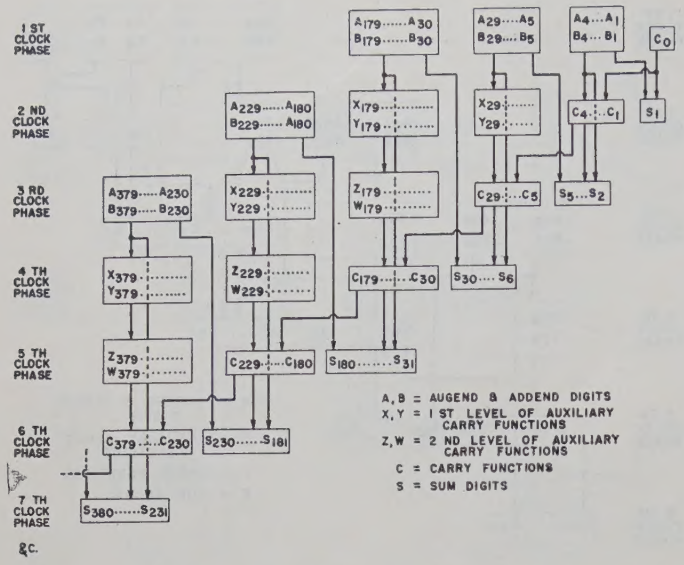

Fig. 9—Formation of parallel groups of sum digits using two levels of auxiliary carry functions.

To show how these carries are formed, the group C_{30} through C_{179} will be considered. The most complicated of these, namely, C_{179}, can be expanded so as to be a function of C_{29} as shown in (11).

$$\left.\begin{aligned} C_{179} = {} & D_{179} + R_{179}D_{178} + R_{179}R_{178}D_{177} + \cdots \\ & + R_{179}R_{178}R_{177} \cdots R_{31}D_{30} \\ & + R_{179}R_{178}R_{177} \cdots R_{30}C_{29} \end{aligned}\right\}. \quad (11)$$

Groups of terms can be combined to form first-level auxiliary carry functions (X's and Y's) as was done previously for the carry expansion shown in Table II. The expansion for C_{179} in terms of the X's and Y's is shown in Table IV. The functions Z are defined as those parts of the terms lying within the small triangles, while the functions W are defined as those parts of the terms lying within the rectangles.

The Z's and W's for C_{179} are written explicitly in Table V. Note that the functions W consist of single terms of six factors each and can be implemented in

TABLE IV

EXPANSION OF C_{179} IN TERMS OF FIRST-LEVEL AUXILIARY CARRY FUNCTIONS AND C_{29}

$C_{179} =$

X_{179}
$+ Y_{179}X_{174}$
$+ Y_{179}Y_{174}X_{169}$
$+ Y_{179}Y_{174}Y_{169}X_{164}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}X_{159}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}X_{154}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}X_{149}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}X_{144}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}X_{139}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}X_{134}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}X_{129}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}X_{124}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}X_{119}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}X_{114}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}X_{109}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}X_{104}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}X_{99}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}X_{94}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}X_{89}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}X_{84}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}X_{79}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}X_{74}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}X_{69}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}X_{64}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}X_{59}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}Y_{59}X_{54}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}Y_{59}Y_{54}X_{49}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}Y_{59}Y_{54}Y_{49}X_{44}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}Y_{59}Y_{54}Y_{49}Y_{44}X_{39}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}Y_{59}Y_{54}Y_{49}Y_{44}Y_{39}X_{34}$
$+ Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}Y_{59}Y_{54}Y_{49}Y_{44}Y_{39}Y_{34}C_{29}$

$C_{179} =$

Z_{179}
$+ W_{179}Z_{149}$
$+ W_{179}W_{149}Z_{119}$
$+ W_{179}W_{149}W_{119}Z_{89}$
$+ W_{179}W_{149}W_{119}W_{89}Z_{59}$
$+ W_{179}W_{149}W_{119}W_{89}W_{59}C_{29}$

TABLE V

EXPRESSIONS FOR SECOND-LEVEL AUXILIARY CARRY FUNCTIONS

$$
\begin{aligned}
Z_{179} &= X_{179}+Y_{179}X_{174}+Y_{179}Y_{174}X_{169}+Y_{179}Y_{174}Y_{169}X_{164}\\
&\quad +Y_{179}Y_{174}Y_{169}Y_{164}X_{159}+Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}X_{154}\\
&= X_{179}+Y_{179}X_{174}+Y_{179}Y_{174}(X_{169}+Y_{169})(X_{169}+X_{164})\\
&\quad +Y_{179}Y_{174}Y_{169}Y_{164}(X_{159}+Y_{159})(X_{159}+X_{154})\\
W_{179} &= Y_{179}Y_{174}Y_{169}Y_{164}Y_{159}Y_{154}\\
Z_{149} &= X_{149}+Y_{149}X_{144}+Y_{149}Y_{144}(X_{139}+Y_{139})(X_{139}+X_{134})\\
&\quad +Y_{149}Y_{144}Y_{139}Y_{134}(X_{129}+Y_{129})(X_{129}+X_{124})\\
W_{149} &= Y_{149}Y_{144}Y_{139}Y_{134}Y_{129}Y_{124}\\
Z_{119} &= X_{119}+Y_{119}X_{114}+Y_{119}Y_{114}(X_{109}+Y_{109})(X_{109}+X_{104})\\
&\quad +Y_{119}Y_{114}Y_{109}Y_{104}(X_{99}+Y_{99})(X_{99}+X_{94})\\
W_{119} &= Y_{119}Y_{114}Y_{109}Y_{104}Y_{99}Y_{94}\\
Z_{89} &= X_{89}+Y_{89}X_{84}+Y_{89}Y_{84}(X_{79}+Y_{79})(X_{79}+X_{74})\\
&\quad +Y_{89}Y_{84}Y_{79}Y_{74}(X_{69}+Y_{69})(X_{69}+X_{64})\\
W_{89} &= Y_{89}Y_{84}Y_{79}Y_{74}Y_{69}Y_{64}\\
Z_{59} &= X_{59}+Y_{59}X_{54}+Y_{59}Y_{54}(X_{49}+Y_{49})(X_{49}+X_{44})\\
&\quad +Y_{59}Y_{54}Y_{49}Y_{44}(X_{39}+Y_{39})(X_{39}+X_{34})\\
W_{59} &= Y_{59}Y_{54}Y_{49}Y_{44}Y_{39}Y_{34}
\end{aligned}
$$

single gating stages. On the other hand, the functions Z, as they appear in the triangles of Table IV, consist of six terms. The first two equations of Table V show how these six-term expressions reduce to four-term expressions which can be implemented in single gating stages.

Substituting Z's and W's into the expression in Table IV, the carry function C_{179} is obtained, which can be reduced from six to four terms as shown in (12).

$$
\left.
\begin{aligned}
C_{179} &= Z_{179} + W_{179}Z_{149} + W_{179}W_{149}Z_{119}\\
&\quad + W_{179}W_{149}W_{119}Z_{89}\\
&\quad + W_{179}W_{149}W_{119}W_{89}Z_{59}\\
&\quad + W_{179}W_{149}W_{119}W_{89}W_{59}C_{29}\\
&= Z_{179} + W_{179}Z_{149}\\
&\quad + W_{179}W_{149}(Z_{119} + W_{119})(Z_{119} + Z_{89})\\
&\quad + W_{179}W_{149}W_{119}W_{89}(Z_{59} + W_{59})(Z_{59} + C_{29})
\end{aligned}
\right\} . \quad (12)
$$

The second expression of (12) can be implemented in a single gating stage one clock phase after the formation of the Z's and W's, and the other 149 carries, C_{178} through C_{30}, can be formed simultaneously as functions of the appropriate Z's and W's and C_{29}. The corresponding sum digits are, of course, formed one clock phase later according to (1).

PRACTICAL EXAMPLE

The foregoing discussions have developed methods for generating many carries simultaneously, and have pointed out the ultimate capability of existing circuitry developments in forming these carries. In the design of an adder in which the number of carries needed simultaneously is less than the possible maximum, a considerable reduction in the number of gating stages needed to generate the auxiliary carry functions can be achieved.

As a practical example, a 53-bit binary adder with two levels of auxiliary carry functions is shown in Fig. 10. Each box in the block diagram represents one gating stage. During the first clock phase the augend and addend are made available as well as C_0. During the second clock phase, C_1 through C_4 are formed directly, as well as the first-level auxiliary carry functions. At the same time, the least significant sum digit, S_1, can be formed. During the third clock phase, C_5 through C_{20} are formed as well as the second level auxiliary carry functions. At the same time the sum digits S_2 through S_5 can be formed. During the fourth clock phase, the rest of the carry functions, C_{21} through C_{52}, are generated and at the same time the sum digits S_6 through S_{21} can be formed. During the fifth clock phase the final sum digits, S_{22} through S_{53}, can be obtained. For use in a complete arithmetic unit, it is usually more convenient to delay the formation of the sum digits S_1 through S_{21} so that the entire sum is obtained in parallel. The sum is, therefore, shown in this manner.

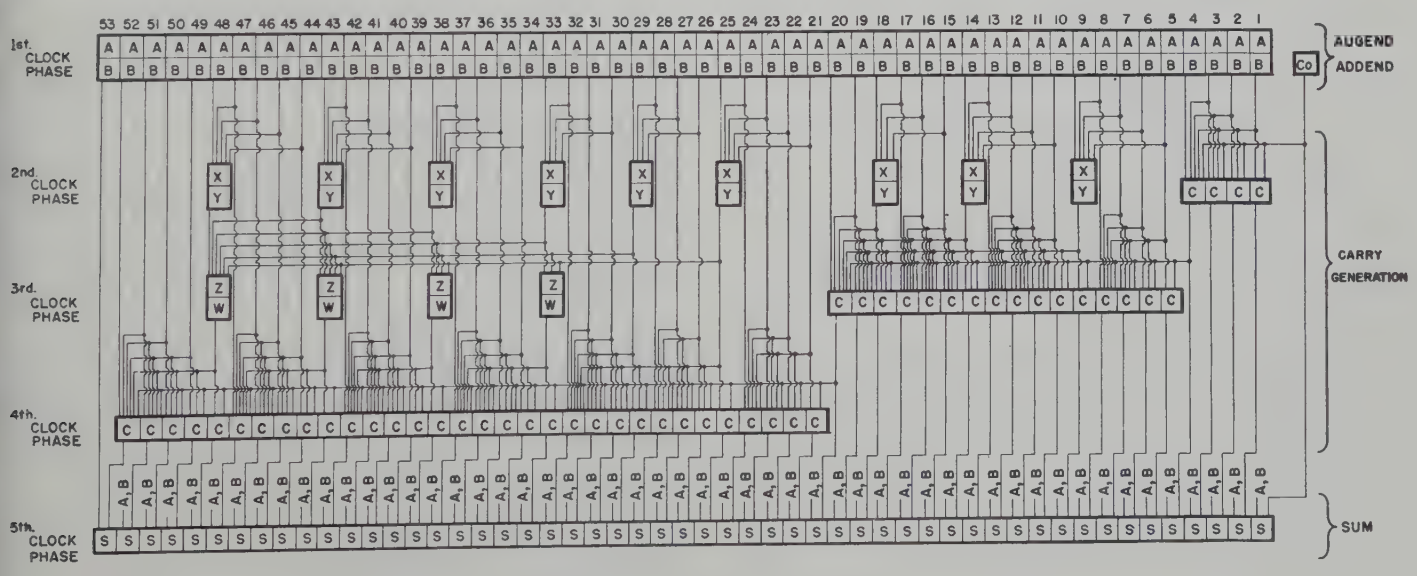

Fig. 10—53-bit parallel binary adder.

TABLE VI

AUXILIARY CARRY FUNCTIONS FOR A 53-BIT PARALLEL BINARY ADDER

F_k REPRESENTS $(A_k+B_k)(A_k+A_{k-1})(A_k+B_{k-1})(B_k+A_{k-1})(B_k+B_{k-1})$; D_k REPRESENTS A_kB_k; R_k REPRESENTS (A_k+B_k)

$X_9 = F_9 + R_9R_8D_7 + R_9R_8R_7D_6 + R_9R_8R_7R_6D_5$	$Y_9 = R_9R_8R_7R_6R_5$
$X_{14} = F_{14} + R_{14}R_{13}D_{12} + R_{14}R_{13}R_{12}D_{11} + R_{14}R_{13}R_{12}R_{11}D_{10}$	$Y_{14} = R_{14}R_{13}R_{12}R_{11}R_{10}$
$X_{18} = D_{18} + R_{18}D_{17} + R_{18}R_{17}D_{16} + R_{18}R_{17}R_{16}D_{15}$	$Y_{18} = R_{18}R_{17}R_{16}R_{15}$
$X_{25} = F_{25} + R_{25}R_{24}D_{23} + R_{25}R_{24}R_{23}D_{22} + R_{25}R_{24}R_{23}R_{22}D_{21}$	$Y_{25} = R_{25}R_{24}R_{23}R_{22}R_{21}$
$X_{29} = D_{29} + R_{29}D_{28} + R_{29}R_{28}D_{27} + R_{29}R_{28}R_{27}D_{26}$	$Y_{29} = R_{29}R_{28}R_{27}R_{26}$
$X_{33} = D_{33} + R_{33}D_{32} + R_{33}R_{32}D_{31} + R_{33}R_{32}R_{31}D_{30}$	$Y_{33} = R_{33}R_{32}R_{31}R_{30}$
$X_{38} = F_{38} + R_{38}R_{37}D_{36} + R_{38}R_{37}R_{36}D_{35} + R_{38}R_{37}R_{36}R_{35}D_{34}$	$Y_{38} = R_{38}R_{37}R_{36}R_{35}R_{34}$
$X_{43} = F_{43} + R_{43}R_{42}D_{41} + R_{43}R_{42}R_{41}D_{40} + R_{43}R_{42}R_{41}R_{40}D_{39}$	$Y_{43} = R_{43}R_{42}R_{41}R_{40}R_{39}$
$X_{48} = F_{48} + R_{48}R_{47}D_{46} + R_{48}R_{47}R_{46}D_{45} + R_{48}R_{47}R_{46}R_{45}D_{44}$	$Y_{48} = R_{48}R_{47}R_{46}R_{45}R_{44}$
$Z_{33} = X_{33} + Y_{33}X_{29} + Y_{33}Y_{29}X_{25}$	$W_{33} = Y_{33}Y_{29}Y_{25}$
$Z_{38} = X_{38} + Y_{38}X_{33} + Y_{38}Y_{33}X_{29} + Y_{38}Y_{33}Y_{29}X_{25}$	$W_{38} = Y_{38}Y_{33}Y_{29}Y_{25}$
$Z_{43} = X_{43} + Y_{43}X_{38} + Y_{43}Y_{38}X_{33} + Y_{43}Y_{38}Y_{33}(X_{29}+Y_{29})(X_{29}+X_{25})$	$W_{43} = Y_{43}Y_{38}Y_{33}Y_{29}Y_{25}$
$Z_{48} = X_{48} + Y_{48}X_{43} + Y_{48}Y_{43}(X_{38}+Y_{38})(X_{38}+X_{33}) + Y_{48}Y_{43}Y_{38}Y_{33}(X_{29}+Y_{29})(X_{29}+X_{25})$	$W_{48} = Y_{48}Y_{43}Y_{38}Y_{33}Y_{29}Y_{25}$

TABLE VII

CARRY FUNCTIONS FOR A 53-BIT PARALLEL BINARY ADDER

F_k REPRESENTS $(A_k+B_k)(A_k+A_{k-1})(A_k+B_{k-1})(B_k+A_{k-1})(B_k+B_{k-1})$; D_k REPRESENTS A_kB_k; R_k REPRESENTS (A_k+B_k)

$C_1 = D_1 + R_1C_0$	$C_{27} = D_{27} + R_{27}D_{26} + R_{27}R_{26}X_{25} + R_{27}R_{26}Y_{25}C_{20}$
$C_2 = D_2 + R_2D_1 + R_2R_1C_0$	$C_{28} = F_{28} + R_{28}R_{27}D_{26} + R_{28}R_{27}R_{26}X_{25} + R_{28}R_{27}R_{26}Y_{25}C_{20}$
$C_3 = D_3 + R_3D_2 + R_3R_2D_1 + R_3R_2R_1C_0$	$C_{29} = X_{29} + Y_{29}X_{25} + Y_{29}Y_{25}C_{20}$
$C_4 = D_4 + R_4D_3 + R_4R_3D_2 + R_4R_3R_2R_1(A_1+C_0)(B_1+C_0)$	$C_{30} = D_{30} + R_{30}(X_{29}+Y_{29})(X_{29}+X_{25}) + R_{30}Y_{29}Y_{25}C_{20}$
$C_5 = D_5 + R_5C_4$	$C_{31} = D_{31} + R_{31}D_{30} + R_{31}R_{30}(X_{29}+Y_{29})(X_{29}+X_{25}) + R_{31}R_{30}Y_{29}Y_{25}C_{20}$
$C_6 = D_6 + R_6D_5 + R_6R_5C_4$	$C_{32} = F_{32} + R_{32}R_{31}D_{30} + R_{32}R_{31}R_{30}(Y_{29}+Y_{29})(X_{29}+X_{25}) + R_{32}R_{31}R_{30}Y_{29}Y_{25}C_{20}$
$C_7 = D_7 + R_7D_6 + R_7R_6D_5 + R_7R_6R_5C_4$	$C_{33} = Z_{33} + W_{33}C_{20}$
$C_8 = F_8 + R_8R_7D_6 + R_8R_7R_6D_5 + R_8R_7R_6R_5C_4$	$C_{34} = D_{34} + R_{34}(Z_{33}+W_{33})(Z_{33}+C_{20})$
$C_9 = X_9 + Y_9C_4$	$C_{35} = D_{35} + R_{35}D_{34} + R_{35}R_{34}(Z_{33}+W_{33})(Z_{33}+C_{20})$
$C_{10} = D_{10} + R_{10}(X_9+Y_9)(X_9+C_4)$	$C_{36} = D_{36} + R_{36}D_{35} + R_{36}R_{35}D_{34} + R_{36}R_{35}R_{34}(Z_{33}+W_{33})(Z_{33}+C_{20})$
$C_{11} = D_{11} + R_{11}D_{10} + R_{11}R_{10}(X_9+Y_9)(X_9+C_4)$	$C_{37} = F_{37} + R_{37}R_{36}D_{35} + R_{37}R_{36}R_{35}D_{34} + R_{37}R_{36}R_{35}R_{34}(Z_{33}+W_{33})(Z_{33}+C_{20})$
$C_{12} = D_{12} + R_{12}D_{11} + R_{12}R_{11}D_{10} + R_{12}R_{11}R_{10}(X_9+Y_9)(X_9+C_4)$	$C_{38} = Z_{38} + W_{38}C_{20}$
$C_{13} = F_{13} + R_{13}R_{12}D_{11} + R_{13}R_{12}R_{11}D_{10} + R_{13}R_{12}R_{11}R_{10}(X_9+Y_9)(X_9+C_4)$	$C_{39} = D_{39} + R_{39}(Z_{38}+W_{38})(Z_{38}+C_{20})$
$C_{14} = X_{14} + Y_{14}X_9 + Y_{14}Y_9C_4$	$C_{40} = D_{40} + R_{40}D_{39} + R_{40}R_{39}(Z_{38}+W_{38})(Z_{38}+C_{20})$
$C_{15} = D_{15} + R_{15}X_{14} + R_{15}Y_{14}(X_9+Y_9)(X_9+C_4)$	$C_{41} = D_{41} + R_{41}D_{40} + R_{41}R_{40}D_{39} + R_{41}R_{40}R_{39}(Z_{38}+W_{38})(Z_{38}+C_{20})$
$C_{16} = D_{16} + R_{16}D_{15} + R_{16}R_{15}X_{14} + R_{16}R_{15}Y_{14}(X_9+Y_9)(X_9+C_4)$	$C_{42} = F_{42} + R_{42}R_{41}D_{40} + R_{42}R_{41}R_{40}D_{39} + R_{42}R_{41}R_{40}R_{39}(Z_{38}+W_{38})(Z_{38}+C_{20})$
$C_{17} = F_{17} + R_{17}R_{16}D_{15} + R_{17}R_{16}R_{15}X_{14} + R_{17}R_{16}R_{15}Y_{14}(X_9+Y_9)(X_9+C_4)$	$C_{43} = Z_{43} + W_{43}C_{20}$
$C_{18} = X_{18} + Y_{18}X_{14} + Y_{18}Y_{14}X_9 + Y_{18}Y_{14}Y_9C_4$	$C_{44} = D_{44} + R_{44}(Z_{43}+W_{43})(Z_{43}+C_{20})$
$C_{19} = D_{19} + R_{19}(X_{18}+Y_{18})(X_{18}+X_{14}) + R_{19}Y_{18}Y_{14}(X_9+Y_9)(X_9+C_4)$	$C_{45} = D_{45} + R_{45}D_{44} + R_{45}R_{44}(Z_{43}+W_{43})(Z_{43}+C_{20})$
$C_{20} = D_{20} + R_{20}D_{19} + R_{20}R_{19}(X_{18}+Y_{18})(X_{18}+X_{14}) + R_{20}R_{19}Y_{18}Y_{14}(X_9+Y_9)(X_9+C_4)$	$C_{46} = D_{46} + R_{46}D_{45} + R_{46}R_{45}D_{44} + R_{46}R_{45}R_{44}(Z_{43}+W_{43})(Z_{43}+C_{20})$
$C_{21} = D_{21} + R_{21}C_{20}$	$C_{47} = F_{47} + R_{47}R_{46}D_{45} + R_{47}R_{46}R_{45}D_{44} + R_{47}R_{46}R_{45}R_{44}(Z_{43}+W_{43})(Z_{43}+C_{20})$
$C_{22} = D_{22} + R_{22}D_{21} + R_{22}R_{21}C_{20}$	$C_{48} = Z_{48} + W_{48}C_{20}$
$C_{23} = D_{23} + R_{23}D_{22} + R_{23}R_{22}D_{21} + R_{23}R_{22}R_{21}C_{20}$	$C_{49} = D_{49} + R_{49}(Z_{48}+W_{48})(Z_{48}+C_{20})$
$C_{24} = F_{24} + R_{24}R_{23}D_{22} + R_{24}R_{23}R_{22}D_{21} + R_{24}R_{23}R_{22}R_{21}C_{20}$	$C_{50} = D_{50} + R_{50}D_{49} + R_{50}R_{49}(Z_{48}+W_{48})(Z_{48}+C_{20})$
$C_{25} = X_{25} + Y_{25}C_{20}$	$C_{51} = D_{51} + R_{51}D_{50} + R_{51}R_{50}D_{49} + R_{51}R_{50}R_{49}(Z_{48}+W_{48})(Z_{48}+C_{20})$
$C_{26} = D_{26} + R_{26}X_{25} + R_{26}Y_{25}C_{20}$	$C_{52} = F_{52} + R_{52}R_{51}D_{50} + R_{52}R_{51}R_{50}D_{49} + R_{52}R_{51}R_{50}R_{49}(Z_{48}+W_{48})(Z_{48}+C_{20})$

If the adder is to be used for multiplication, division, and other operations requiring the recirculation of the sum digits back into one of the inputs, five clock phases are necessary in order to complete the addition as well as the recirculation in one microsecond.

The expressions for the auxiliary carry functions as well as the final carry functions for this example are shown in Tables VI and VII, respectively. Note that the factors D, R, and F are merely mathematical abbreviations representing certain combinations of A's and B's, as shown in the table headings. The X's, Y's, Z's, W's, and C's are similar to the ones shown in the previous examples. In this case, however, the final carries, C_5 through C_{52}, are formed not as functions of only the auxiliary carry functions and the last carry from the previous clock phase, but as functions of a combination of auxiliary carry functions, augend and addend digits, and the last carry from the previous clock phase. This arrangement reduces the number of auxiliary carry functions to a reasonable proportion. In addition to the four registers of gating stages for the augend digits, addend digits, carry functions, and sum digits, only 26 gating stages, equivalent to one half of a register, are required to create the auxiliary carry functions.

A Small Coincident-Current Magnetic Memory*

W. J. BARTIK† AND T. H. BONN†

Summary—**This paper describes a small coincident-current memory used for buffer storage. Such a memory as part of the self-checking card-to-magnetic-tape converter, an auxiliary of the Univac System, is now in production. Typical advantages of a small coincident-current memory in computer input-output equipment, as well as some of the problems encountered in its application, are described.**

This memory affords the card-to-tape converter a great degree of flexibility, making it possible to read cards sidewise and to check and edit information with a minimum of hardware and complexity.

Memory cells consist of metallic-tape cores wound with multiturn coils. The low currents required permit operation of the memory directly from the card-sensing brushes on writing and from a diode function-table on reading.

The functional aspects of the memory and its associated electrical circuitry are described. Information concerning the physical nature of the memory, specifications of the cores, and some of the tests performed in their inspection is also presented.

Introduction

A NUMBER of papers have previously described large coincident-current memories employing rectangular-hysteresis-loop magnetic materials.[1] This paper describes a small coincident-current memory used as an important part of the self-checking card-to-tape converter[2], an auxiliary unit of the Univac System. Some of the advantages of small memories in a typical buffer-storage application, as well as some of the problems encountered, are described here.

The memory can store 960 bits, the total number of bits possible on a punched card (80 columns by 12 rows). Each storage cell is a metallic-tape core with 3 windings. Currently in production for the card-to-tape converter, the memory is the first such device to be made for commercial equipment.

System Discussion of the Card-to-Magnetic-Tape Converter

The card-to-magnetic-tape converter transfers information from punched cards to the magnetic tape used in the Univac System. Storage of information within the converter is required for these reasons: 1) In effect, the memory serves as a device to rotate each card ninety degrees. The cards are read sidewise in order to obtain the maximum card-reading rate with a given card velocity. Thus card information is available to the machine row by row, but for use by Univac it must be recorded on the magnetic tape column by column, that is, one complete digit at a time; 2) The memory is used in conjunction with a plugboard to edit and rearrange the information from cards; 3) The memory is a part of the self-checking circuits of the converter.

The memory is a matrix of magnetic cores arranged in 80 columns[3] and 12 rows. The 80 columns of the memory correspond to the 80 columns of a punched card and the 12 rows of the memory correspond to the 12 rows of the card. Thus there is a corresponding core in the memory for every possible hole in the card. Each core has three separate windings, designated as the row winding, the column winding and the readout winding.

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I. L. Auerbach, "A static magnetic memory system for the ENIAC," *Proc. Assn. for Computing Machinery*, pp. 213–222; May, 1952.

[2] E. I. Blumenthal, "A self-checking card-to-magnetic-tape converter," presented at AIEE Winter general meeting, 1955.

[3] Both 90-column and 80-column models of the machine are available.

Information is stored in a particular core in the memory by simultaneous excitation of its column winding and its row winding.

The operation of the converter is illustrated in Fig. 1. As the card enters the card-feed unit, its front edge interrupts a photocell beam to produce a leading-edge pulse, which synchronizes the pulsing of the memory with the movement of the card. An array of brushes senses the holes in the card. The entire brush array is pulsed by a common source which sends current through any column whose corresponding hole is under the brush. The brush pulser pulses synchronously with each of the 12 rows of the card as they travel under the card-feed brush. During this period the leading-edge pulse generates 12 pulses which are applied to the row windings synchronously with the column excitation and movement of the card.

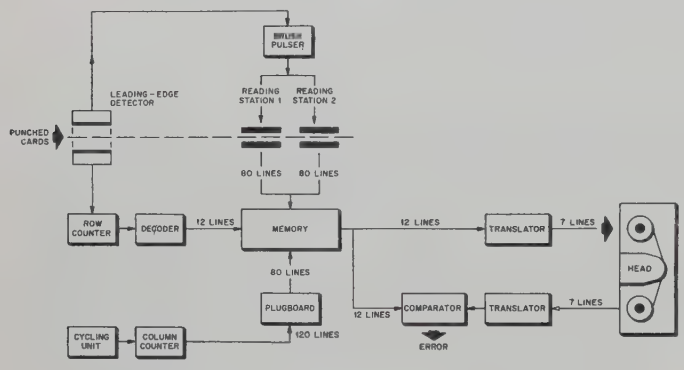

Fig. 1—Operation of the card-to-tape converter.

Coincidence of column and row currents at a core switches the core to store a binary 1. When either the row current or the column current is present by itself, the core is not switched but is left with a binary 0.

Information is read from the memory by means of a cycling unit, a column counter, a 16-line encoder, an 8-line encoder, a 120-line encoder, and a plugboard. The cycling unit supplies timing pulses for the machine; the counter counts cycling-unit pulses and the decoders decode the counter outputs to produce 120 individual pulses with a width of 40 microseconds each and a period of 80 microseconds. Eighty of these pulses are applied to the column windings to read out of the memory. Upon completion of the 80 readout operations the extra 40 pulses produce 40 fill-digits on the magnetic tape to complete a 120-digit blockette required by the Univac System. During the read-out operation the plugboard controls the sequence in which information is read out of the memory and recorded on tape.

In some cases, it is desirable to edit the card information by performing a column split in reading from the memory. When a column is split, part of it is read the first time the column is passed, the remaining portion when the column is passed the second time. This is done by inhibiting row windings corresponding to the parts of the column which are not to be read synchronously with the column read-out pulse. For editing a commercial problem complete independence or freedom of the column-split operation is not required. It is sufficient to inhibit either the first two memory rows corresponding to the first two card rows, which contain alphabetic-control information, and/or the ten rows of memory corresponding to the last ten rows of the card, which contain numerical information.

It is possible to inhibit the alphabetic-row information for 12 columns and the numerical-row information for 12 columns. The information from the inhibited row may be read out by using 24 of the extra 40 read-out pulses. The number 24 is fixed by the number of columns which may be required to be split and not by any logical design considerations.

The memory is a vital link in self-checking operations of the machine. The punched card passes through two brush stations. At the first station the information on the card is stored in the memory. The information is subsequently read out of the memory, translated into Univac code, and recorded on tape in a sequence determined by the plugboard. As the punched card passes the second station, the memory is filled a second time, using a second set of brushes. During this pass, rows 1 and 2 of the memory are interchanged and rows 3 through 12 are permutated. This is done rather than permutating all 12 rows because of the way in which the columns are split. Then, in a verification run, the new contents of the memory are compared, digit by digit, with information as it is read back from the tape which had been reversed and is now running in the normal direction. If there is disagreement, the machine stops and an appropriate indicator lights. With this check, existence of an undetected error is practically impossible.

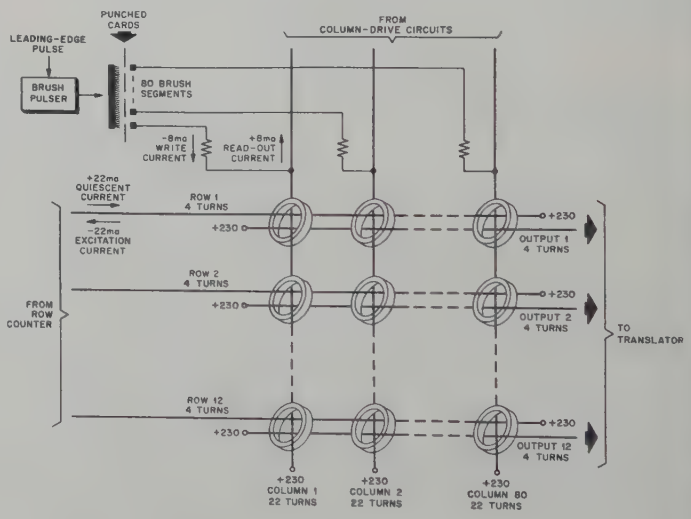

Fig. 2—Magnetic-core memory.

Electrical Description of the Memory

The memory (Fig. 2) consists of a magnetic-core matrix arranged in 80 columns and 12 rows. A column winding of 22 turns runs through each of the 80 col-

umns; two row windings of 4 turns each run through each of the 12 rows. One of these row windings is driven, the other is an output winding. A bias value of +88 milliampere-turns is kept on each core by a quiescent column current of zero and a quiescent row current of +22 milliamperes. The value of 88 milliampere-turns is referred to as +1/3 unit-excitation in Fig. 3.

MMF				ACTION
QUIESCENT	ROW	COLUMN	NET	
+1/3	-2/3	-2/3	-1	STORE BINARY 1
+1/3	-2/3	0	-1/3	STORE BINARY 0
+1/3	0	-2/3	-1/3	STORE BINARY 0
+1/3	0	+2/3	+1	READ
+1/3	-2/3	+2/3	+1/3	DO NOT READ (INHIBIT READOUT)

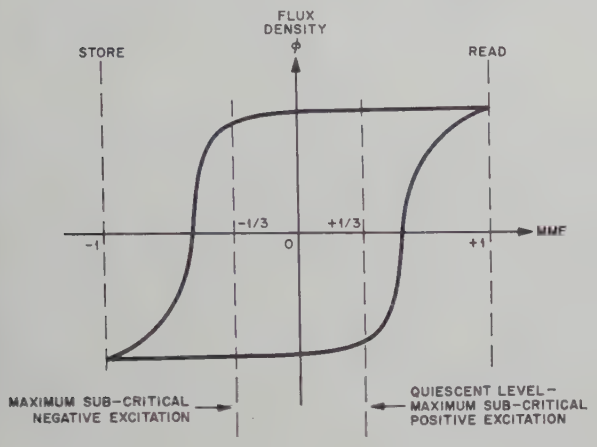

Fig. 3—Excitation levels, with hysteresis loop.

The various excitation levels and a hysteresis loop are shown in Fig. 3. The hysteresis loop of the memory cores is such that a total magnetomotive force change of −4/3 units from the bias point of +1/3 unit stores a binary 1 in the core. A total change of +2/3 unit from the bias-point causes information to be read out of the core.

The −4/3 units required to store a 1 is obtained by the coincidence of −2/3 unit from the column winding (−8 milliamperes through 22 turns) and −2/3 unit from the row winding (−44 milliamperes through four turns). Either of these signals alone result in a net excitation of −1/3 unit on the core, which is not sufficient to store a 1. The +2/3 unit required to read is supplied by the column winding (+8 milliamperes through 22 turns). If a readout is to be inhibited, a −2/3 unit excitation is supplied by the row winding before the column-read-out signal. The total excitation when the column-read-out signal is applied is then +1/3 unit, which will not read out the core.

The ratio of the total magnetomotive force at the selected core to the maximum magnetomotive force at any unselected core is 3/1 for either reading or storing. This is the largest value of this ratio that can be obtained with a two-dimensional memory. A large value for this ratio is desirable for two reasons. First, it reduces the degree of rectangularity required of the core-material hysteresis loop. A rectangular loop is necessary to obtain small outputs for those currents which do not select the core. Second, it reduces the regulation requirement on the driving currents.

The speed of the memory is compatible with the rest of the converter. The period between successive storage operations is four milliseconds, two of which are actually used for storage. The two-millisecond period is the maximum time that the brush can remain in a hole in the card and allow current to flow through the memory. The period between successive read operations is 80 microseconds, forty of which are required for the actual reading. Forty microseconds is the time the column-read current is on. The core responds in a maximum time of 23 microseconds in either storing or reading.

Drive Circuits

The circuit which drives the column windings is shown in Fig. 4. The column-store signal is provided by the brush pulser which produces a regulated pulse of 80-volts amplitude. The 80-volt signal is converted to an 8-milliampere current by a 10,000-ohm resistor in series with it. The column-read signal is provided by the combined outputs of the 16-line decoder and the 8-line decoder.

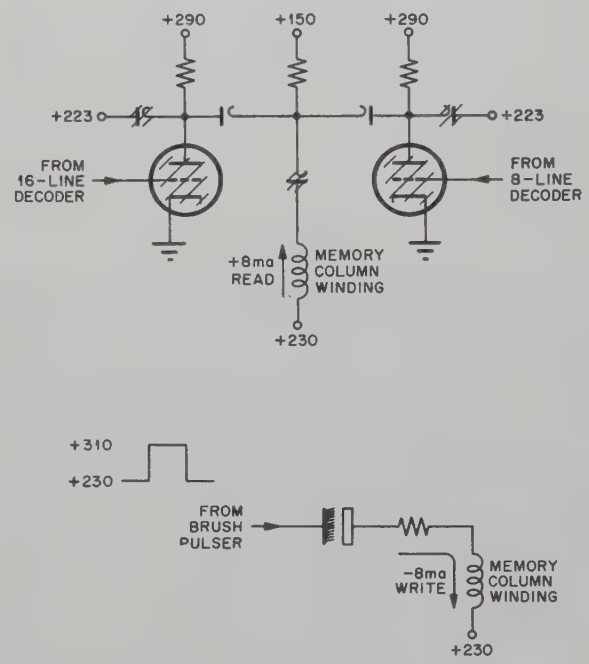

Fig. 4—Driving circuit for column windings.

The row-drive circuit is shown in Fig. 5. This represents a typical information row where a quiescent current of +22 milliamperes and a pulsed current of −22 milliamperes flow. All currents in the memory are stable in amplitude to ±5 per cent.

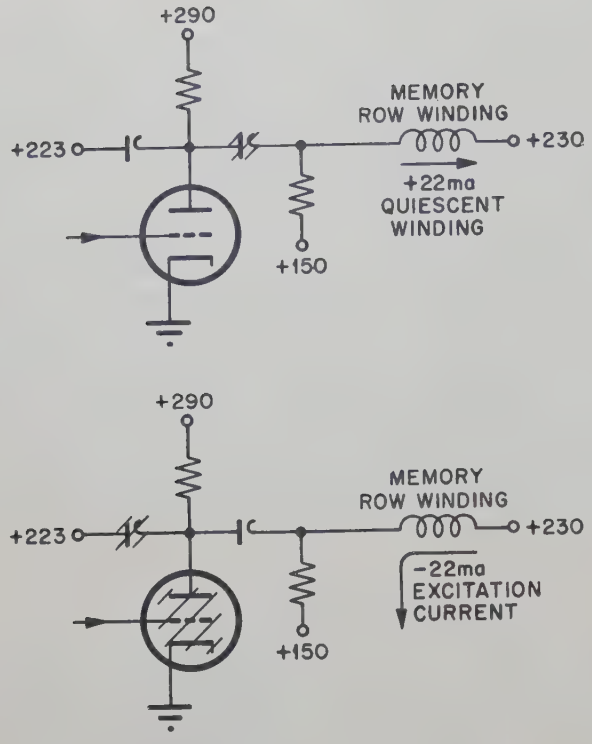

Fig. 5—Drive circuit for row winding.

Output Amplifier

The 4-turn output-winding of the memory furnishes a nominal 1-signal of 60-millivolt peak-amplitude. The signal is amplified to a useful level by an integrating amplifier. Integration is performed in preference to sampling for four reasons: 1) The integrated output of the core does not change with exciting-current rise time; 2) Integration makes the output less dependent on small variations in the coercive force from core to core. The core must still be operable under coincident-current conditions but the actual change in shape and duration of the 1-output, which is related to the coercive-force variations, is not of importance; 3) The range of 1-outputs is less; 4) Core-material hysteresis-loop requirements are less stringent.

The amplifier circuit is shown in Fig. 6. The input signal to the amplifier is transformer-coupled to the amplifier to obtain a voltage gain of 10. The signal is amplified further in an integration amplifier which consists of tubes V_1 V_2, and V_{3a} shown in Fig. 6. The integration action is accomplished in the feedback network from the cathode of V_{3a} to the cathode of V_1.

The integrated output of the amplifier is cleared by means of a double-ended keyed clamping arrangement. The outputs of the amplifiers are unclamped and are permitted to rise for only 35 microseconds after the reading operation commences. The use of the keyed clamp minimizes the hum problem in the amplifier since it is responsive to a 60-cycles-per-second input for only a small fraction of a cycle. The transformer coupling is nonperfect and produces a quasi-differentiated signal. This quasi-differentiation ensures that the response of the transformer to a 1- or a 0-signal will be substantially over in 80 microseconds, the period of the read-out signals. Resistors are placed in series with the transformer primary to control the time constant. Because of the quasi-differentiation of the input circuit, the amplifier produces a quasi-integrated output, however, the advantages of integration cited above obtain.

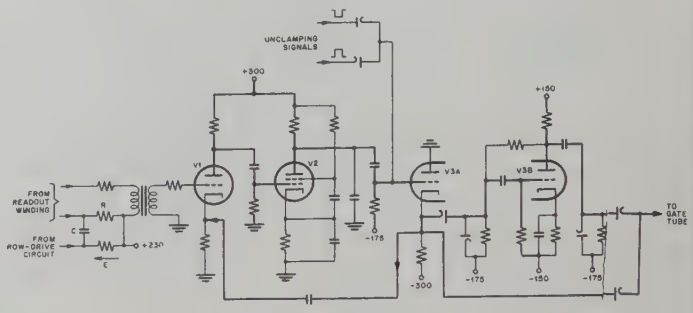

Fig. 6—Integration amplifier.

Whenever a row is inhibited, a spurious output pulse from that row is generated. Two factors minimize the effect of this spurious pulse. First, the polarities of the output windings are so arranged that the output voltages of adjacent cores in a row alternate in sign. Second, to aid further in minimizing this spurious signal a signal developed across a resistor R in series with the row drive line is differentiated and fed into the transformer primary. Complete cancellation of this spurious signal, V_p, is possible when the following equations are satisfied:

$$RC\frac{dE}{dt} = V_p, \quad \text{or} \quad RCE = \int V_p dt.$$

The amplitude of V_p depends upon the particular information pattern stored in a row of cores. But this is not objectionable in practice because the subcritical magnetomotive force which is only $\frac{1}{3}$ that of the exciting magnetomotive force produces an output which is very nearly the same whether a 1 or a 0 is stored in the core.

Because of the alternation in polarity of the memory outputs the amplifier is designed to accept bi-directional signals. The bi-directional signals are divided into two paths—one path leading from the cathode of V_{3a} to the output; the other path through an inverter V_{3b} and then to the output. The output is presented to the suppressor grid of a gate tube. The control grid of the gate is pulsed for 15 microseconds, starting 10 microseconds after the onset of the read-current pulse.

The amplifier must also tolerate some very large overload signals during the store operation. The largest signal occurs when forty 1's are stored in alternate cores in a row of the memory since the voltage of the output line has the same polarity for each 1. Since at least 1 millisecond is available after the end of the store operation before the read operation starts, this signal has ample time to decay.

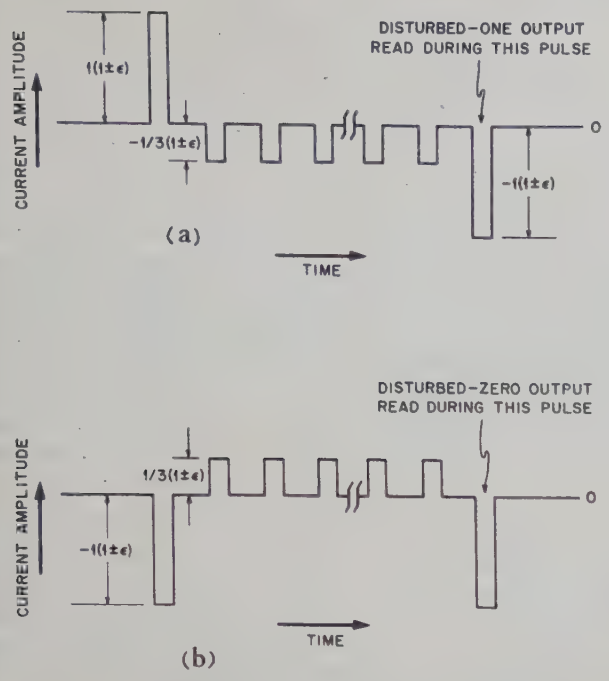

Fig. 7—(a) Pulse pattern to obtain a disturbed one. (b) Pulse pattern to obtain a disturbed zero.

Core Specifications and Tests

Specifications for memory cores were based on tests performed on an initial shipment of cores. The cores were tested with two types of pulse patterns as shown in Figs. 7(a) and 7(b). The pattern in Fig. 7(a) results in a disturbed-one output and that of Fig. 7(b) in a disturbed-zero output.

In initial tests the tolerances on the storing and reading currents were investigated to determine that configuration of tolerances which result in the severest test of the core. It was assumed that the magnitude of the tolerance ϵ shown in Figs. 7(a) and 7(b) was the same for storing, inhibiting, and reading pulses, but that the sign of ϵ may differ. All the possible current patterns which result when this convention is followed were investigated. It was found that the two patterns which gave the most extreme outputs were: 1) Reading and storing currents which are ϵ per cent less than their nominal amplitude and the inhibiting currents which are ϵ per cent greater than their nominal amplitude. This pattern will give the largest disturbed-zero and inhibited outputs, the smallest disturbed-one output and the longest switching time; 2) Reading and storing currents which are ϵ per cent greater than their nominal amplitude and the inhibiting pulse absent. This pattern will give the largest 1-output and the fastest switching time. As a matter of convenience and ease the actual pattern chosen for production testing has the reading and storing currents ϵ per cent greater than their nominal amplitude and the inhibiting pulse ϵ per cent greater than its nominal value. This pattern will very nearly give the same 1-output and switching time as the pattern with the inhibiting pulse absent.

With the value of ϵ set at 10 per cent the core outputs must meet the following specification for the two tolerance configurations listed previously: 1) The 1-output must be greater than 55 millivolt-microseconds, but less than 80; 2) The duration of the 1-output measured to the point where 95 per cent of the flux change has occurred must be between 5 and 23 microseconds; 3) The 0-outputs and inhibiting outputs must be less than 5 millivolt-microseconds.

Physical Description of Memory

The cores are made of five wraps of 4–79 Moly-Permalloy tape $\frac{1}{8}$ mil thick and $\frac{1}{8}$-inch wide, wound on 3/16-inch diameter steatite bobbins. Fig. 8 shows several of these cores and gives an indication of their size.

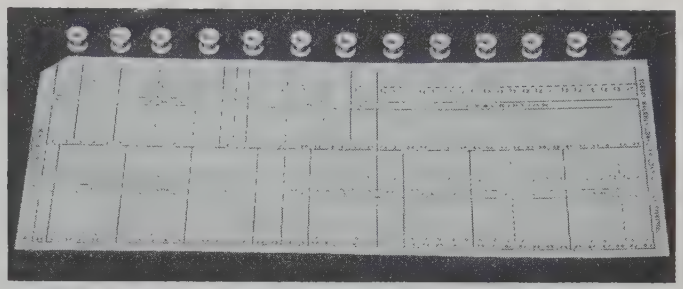

Fig. 8—Memory cores.

Ten cores are mounted in a bakelite block (Fig. 9) and a bakelite cover is placed over them. The block and the cover are suitably grooved to accommodate the windings. The row winding is connected to the two inside pins and the output winding is connected to the two outside pins. Placing the cores in a block and treating the assembly as a unit minimizes handling and possible damage to the strain-sensitive metallic-tape cores.

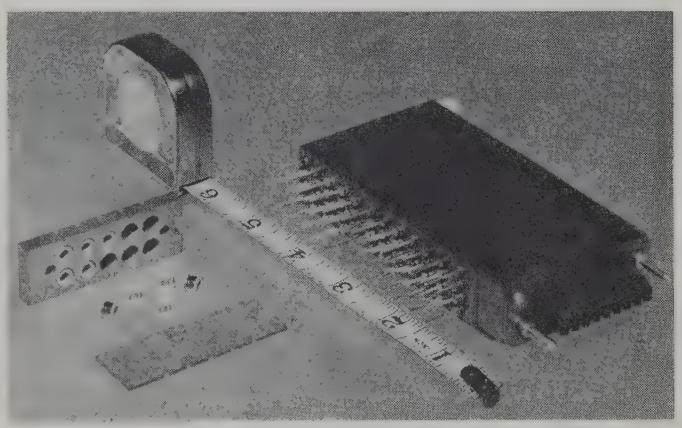

Fig. 9—Complete memory section.

The 4-turn row winding and the 4-turn output winding are wound through the grooves and link each of the 10 cores. The ends of the windings are brought out to four pins in the ends of the block.

After the row and read-out windings are completed, the blocks are stacked 12 high so that the core holes and edge grooves are lined up. Twenty-two turns of wire are run through each column of 12 core holes. The turns are guided on their return trip through grooves in the edge of the block in order to keep the entire winding below the surface. The ends of the 10-column windings are then wired to a commercial connector. After all winding and wiring to connectors is completed, the two wide sides of the memory section are covered with bakelite sheets to protect the windings. The complete section is shown in Fig. 9.

Eight of these sections connected together make up a complete memory matrix of 80 columns by 12 rows. The eight sections of the memory plug into mating connectors in the supporting bracket shown in Fig. 10.

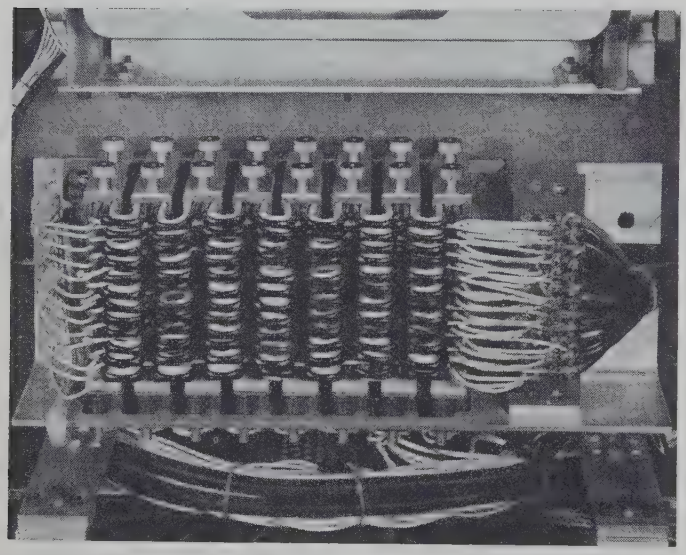

Fig. 10—Eight complete memory sections mounted in the card-to-tape converter.

Jumpers connect the row and output windings of blocks of adjacent sections in series. The entire memory is housed in a mu-metal shield to protect the components from physical shock and to shield them from external magnetic fields. This shielding was found to be important because the memory is mounted close to large chokes and transformers in the card-to-magnetic-tape converter.

Conclusion

As of this date, twenty card-to-tape converter units have been built and all have worked satisfactorily. Some have been in the field for as long as two years. No errors made during this time have been ascribable to the memory.

The general approach to the use of metallic-tape cores and multiturn windings differs from the usual approach where ferrite single-toroids with single-turn windings are driven by a vacuum tube or a transformer, or both. At the time that this particular memory development started, satisfactory ferrite toroids were not available. Therefore, attention had to be focused on the available metallic-tape toroids. The metallic-tape cores require less magnetomotive force and are easier to drive than ferrite cores. The development of low coercive-force ferrites has, however, reopened the question of metals vs ferrites.

The small size of the memory with its relatively large number of edge connections (92) indicated that a single-turn approach would require a larger number of relatively high-powered and expensive driving circuits. For this reason it was decided to use more than one turn on the cores so that the column windings could be driven by an ordinary crystal-diode matrix and the row windings by a small power tube (25L6). It is believed that the winding time involved in constructing the memory is less than the cost of the drivers for driving a memory in which single-turn coils are used.

Dividing the memory into 8 sections simplifies construction because memory sections can be easily interchanged to check for possible memory failures. Faulty units can be easily removed for repair.

The use of a 3/1 ratio of exciting magnetomotive force to maximum subcritical magnetomotive force has made the core requirements reasonably uncritical at a negligible extra expense.

Acknowledgment

Among those other than the authors who contributed to the development described herein are G. C. Gingrich, R. P. Talambiras, and J. D. Lawrence, Jr. E. I. Blumenthal was project engineer on the over-all card-to-tape converter program.

Reflected Number Systems*

IVAN FLORES†

Summary—**Many papers have been written about the reflected binary system and it is well known in the computer field for analog-to-digital conversion. The method used in creating this system may be extended to systems of bases other than two. It is the purpose of this paper to carry this extension to its logical conclusion. The author describes how reflected systems of different bases may be composed. The equations for translating between the conventional and reflected systems are then derived. It is also demonstrated how the reflected binary system is a special case of reflected number systems and how the general case simplifies for the reflected binary case.**

Introduction

THE PROPERTIES of integers and the process of counting are independent of the number system in use. The Hindu-Arabic or decimal system with which we are so familiar is as good as any. Systems with other bases, such as the binary and octal systems have some special importance in their application to computers. The scales of notation and the methods of translation from one base to another may be reviewed in a basic book on number theory as that of Uspensky and Heaslet.[1] The applications to computers may be reviewed in books by Engineering Research Associates and R. K. Richards.[2,3]

As the applications for computers increased the problem of analog-to-digital conversion arose. It is exceedingly difficult to solve this problem within the framework of conventional number systems. To that end, the reflected binary or Gray code was invented by F. Gray.[4] This code has had many applications in industry and computer work.[5–8]

This paper treats the reflected number system generalized to any base and considers the conversion of the conventional number to the reflected number and vice versa.

Theory

In current automatic calculators, it often becomes necessary to read in digital form a continuously varying quantity. In the transitional case difficulty arises. When several digits change at once, if the reading method is imperfect, ambiguities may arise. To examine an example in decimal notation, suppose it is desired to digitalize to four figures an analog quantity when the quantity to be digitalized lies between 1,999 and 2,000. If there is no mechanism to block out an intermediate reading, a mechanical device might read some of the digits as changed and not others. Thus it could read 2,999 or 1,000 or 1,909 or one of many other combinations. A reflected number system eliminates such an eventuality.

In a reflected system, never more than one digit changes at one time. To see how this can be done, let us call the largest digit L, in a system under consideration with base B. Then $L=B-1$, for the base is never one of the digits in the system. Counting proceeds from 0 to L. Call a number system using a natural number as a base a conventional system. In such a system the next number after L would be 10. This would mean that two digits change simultaneously. Considering L as $0L$ in the reflected system, the next number after L is $1L$. The number after that is formed by reducing the right hand digit. After $1L$ we have $1(L-1)$. We continue decreasing this last digit until we reach 10 (after 11). The next number is 20 (in any but the reflected binary system). We must now increase the right hand digit so that the next number after 20 is 21. Table I shows a comparison of the decimal, octal, and reflected octal systems.

TABLE I
A Comparison of the Decimal, Octal, and Reflected Octal Number Systems

Decimal	Octal	Reflected Octal
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	10	17
9	11	16
10	12	15
11	13	14
12	14	13
13	15	12
14	16	11
15	17	10
16	20	20
17	21	21
18	22	22
19	23	23
20	24	24
21	25	25
22	26	26
23	27	27
24	30	37
25	31	36

* Manuscript received by the PGEC, May 27, 1955; revised manuscript received February 6, 1956.
† Nuclear Development Corp. of America, White Plains, N.Y.
[1] J. V. Uspensky and M. A. Heaslet, "Elementary Number Theory," McGraw-Hill Book Co., Inc., New York; 1939.
[2] Engineering Research Associates, "High Speed Computing Machines," McGraw-Hill Book Co., Inc., New York; 1950.
[3] R. K. Richards, "Arithmetic Operations in Digital Computers," D. Van Nostrand and Co., New York; 1955.
[4] F. Gray, "Pulse Code Communication," Patent 2,632,058, March 17, 1953.
[5] F. A. Foss "The use of a reflected code in digital control systems," Trans. IRE, vol. EC-3, pp. 1–6; December, 1954.
[6] H. J. Gray, Jr., P. V. Levonian, and M. Rubinoff, "An analog-to-digital converter for serial computing machines," Proc. IRE, vol. 41, pp. 1462–1465; October, 1953.
[7] R. E. Yaeger, "The Gray-to-binary translator and shift register," *The Transistor*, pp. 611–626; November, 1951.
[8] W. Goodall, "Television by pulse code modulation," *Bell Syst. Tech. J.* vol. 30, pp. 38; January, 1951.

We continue counting as described above. If the units, digit is decreasing we change the tens' digit at the next count after the units' digit becomes 0; if the units' digit is increasing we change the tens' digit after the units' digit reaches L. After the tens' digit increases to L we change the hundreds' digit. When the tens' digit changes we continue to count by now counting the units' digit in the opposite direction. This is much more complicated to describe than demonstrate. Table II shows counting in the decimal, quaternary, and reflected quaternary systems.

TABLE II

A Comparison of the Decimal, Quaternary, and Reflected Quaternary Number Systems

Decimal	Quaternary	Reflected Quaternary
0	0	0
1	1	1
2	2	2
3	3	3
4	10	13
5	11	12
6	12	11
7	13	10
8	20	20
9	21	21
10	22	22
11	23	23
12	30	33
13	31	32
14	32	31
15	33	30
16	100	130
17	101	131
18	102	132
19	103	133
20	110	123
21	111	122
22	112	121
23	113	120
24	120	110
25	121	111
26	122	112
27	123	113
28	130	103
29	131	102
30	132	101
31	133	100
32	200	200
33	201	201

Let us try to find a way of translating from a reflected system to its conventional counterpart. Call the base B, as before, and the digits in the reflected system, $a_n, a_{n-1}, \cdots, a_2, a_1$, reading from left to right. The digits of the same number written in the conventional system of base B are $A_n, A_{n-1}, \cdots, A_2, A_1$. We shall use induction to find the equation.

For a one digit number, $A_1 = a_1$.

For a two digit number, $A_2 = a_2$. But now if a_2 is even then $A_1 = a_1$; if $a_2 =$ is odd, then $A_1 = L - a_1$, for then we count downwards from L. In other words, A_1 is the L's complement of a_1.

For a three digit number, $A_3 = a_3$. If a_3 is even, $A_2 = a_2$; if a_3 is odd, $A_2 = L - a_2$. If a_3 and a_2 are both even or both odd, $A_1 = a_1$; if one of them is even and the other odd, $A_1 = L - a_1$. If both are even we are counting forward with the last digit; if both are odd we have changed our direction of counting twice and so are also counting forward, if one of a_3 and a_2 is odd and the other is even, we have reversed counting just once and so we must take the L's complement of a_1.

In mathematical symbols the condition that a number, N, is even is written, $0 = N \pmod 2$. This means there is no remainder when N is divided by two, the definition of an even number. $1 = N \pmod 2$ indicates an odd number which has a remainder of one when N is divided by two. Hence $N \pmod 2$ is one for odd numbers and zero for even numbers.

For a two digit number let $e_1 = a_2 \pmod 2$ which means e_1 is the remainder when a_2 is divided by 2. Then $A_1 = e_1 L + (-1)^{e_1} a_1$.

For a three digit number let $e_2 = a_3 \pmod 2$ and $e_1 = (a_3 + a_2) \pmod 2$. Then e_1 will be zero for both a_3 and a_2 even or both odd; otherwise e_1 will be one. Now $A_2 = e_2 L + (-1)^{e_2} a_2$, and $A_1 = e_1 L + (-1)^{e_1} A_1$. For the general case of an n digit number in the reflected system with base B we have:

$$
\begin{aligned}
A_n &= a_n, \\
A_{n-1} &= e_{n-1} L + (-1)^{e_{n-1}} a_{n-1}; \\
e_{n-1} &= a_n \pmod 2, \\
&\cdots\cdots\cdots\cdots \\
A_{n-k} &= e_{n-k} L + (-1)^{e_{n-k}} a_{n-k}; \\
e_{n-k} &= (a_n + a_{n-1} \cdots + a_{n-k+1}) \pmod 2, \text{ etc.} \\
&\cdots\cdots\cdots\cdots
\end{aligned}
$$

This may be written:

$$A_k = e_k L + (-1)^{e_k} a_k, \qquad k = 1 \text{ to } n \quad (1)$$

$$e_k = \sum_{i=k+1}^{n+1} a_i \pmod 2 \qquad k = 1 \text{ to } n \quad (2)$$

Note that $a_{n+1} = 0$ and hence e_n is zero.

This relation is true whether the base B is odd or even. That is an interesting fact because the transition of the left hand digit in an odd based system always occurs with the right hand digit increasing. In contrast, the even based system may have the right hand digit either increasing or decreasing when the left hand digit is in transition.

It is now desired to translate from a conventional system with base B to the equivalent reflected system of the same base. This could be done by solving (1) for a_k. This would involve complicated expressions with exponents that are summations. It is easier to examine the cases of odd and even bases separately.

Odd Base

Before examining the translation between numbers in systems with odd bases, let us make this observation. The complement of the digit α is $L - \alpha$. When the base B is odd, L is consequently even, being one less than B.

This leads to:

$$\begin{aligned}(L-\alpha) \pmod 2 &= L \pmod 2 - \alpha \pmod 2 \\ &= \alpha \pmod 2 \\ &= \alpha \pmod 2. \end{aligned} \tag{3}$$

The complement of a digit in an odd base system is thus even or odd only if the digit is respectively even or odd. Let us examine (1).

Remember either

$$a_i = A_i \text{ or } a_i = L - A_i.$$

But in either case,

$$a_i \pmod 2 = A_i \pmod 2. \tag{4}$$

Therefore,

$$e_k = \sum_{i=k+1}^{n+1} A_i \pmod 2. \tag{5}$$

From (2), if $e_k = 0$ then $A_k = a_k$; if $e_k = 1$ then $A_k = L - a_k$. This may be written as:

$$a_k = e_k L + (-1)^{e_k} A_k. \tag{6}$$

What may be deduced from (5) and (6) is that if y is some conventional odd base number whose reflected representation is X then the conventional number x (written with the same digits as X) translates in to the reflected number Y. As an example 141 in conventional quinary is 103 in reflected quinary and 103 in conventional quinary is 141 in reflected quinary.

Even Base

In converting from a conventional to a reflected system, whether a digit is complemented or not depends on the number of multiples of the next higher power of the base which is contained in the conventional number. It is a function of whether this multiple is even or odd. The multiple of the next higher power of the base is a multiple of the base plus the digit to the left of the one in question. Since an even base is being considered, only the digit to the left of the one in question determines this complementation. For instance, the fourth reflected digit from the left will be the same as the fourth conventional digit if the third conventional digit is even; it will be the complement of the fourth conventional digit if the third is odd.

This can be put into mathematical notations:

$$a_k = e_k L + (-1)^{e_k} A_k \tag{7}$$

$$e_k = A_{k+1} \pmod 2 \tag{8}$$

(5), (6), (7), and (10) may be summarized in one set of equations:

$$a_k = e_k L + (-1)^{e_k} A_k \tag{9}$$

$$e_k = (A_{k+1} + e_{k+1} B) \pmod 2. \tag{10}$$

Now any number in a conventional system with any base B may be translated into the corresponding number in the reflected system with the same base B.

It might prove fruitful to show how the derivation applies to the binary system. The reflected binary system is currently in use for analog-to-digital encoding and also carries the name *Gray Code*. It would therefore be convenient to be able to translate from reflected to conventional binary and back. Eqs. (1) and (2) hold, of course, but they may be simplified. Since we are in a binary system, the digits are all one or zero and we may do our adding more directly (mod 2). Also zero and one are L-complements of each other. So we have $L=1$ and, since $A-B \pmod 2 = A+B \pmod 2$, then:

$$A_k = e_k \cdot 1 + a_k \pmod 2 = \sum_{i=k}^{n+1} a_i \pmod 2. \tag{11}$$

In words, to find the conventional binary digit in the k position, add the reflected binary digits in positions k to n, divide by two and keep only the remainder. See Table III to get a better idea of the process.

TABLE III

A Comparison of the Decimal, Binary, and Reflected Binary Number Systems

Decimal	Binary	Reflected Binary
0	0	0
1	1	1
2	10	11
3	11	10
4	100	110
5	101	111
6	110	101
7	111	100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000
16	10000	11000
17	10001	11001
18	10010	11011
19	10011	11010
20	10100	11110

To translate from conventional to reflected binary we may manipulate (11):

$$A_k = \sum_{i=k}^{n+1} a_i \pmod 2 = \sum_{i=k+1}^{n+1} a_i + a_k \pmod 2 \tag{12}$$

$$a_k = A_k - \sum_{i=k+1}^{n+1} a_i \pmod 2 = A_k + \sum_{i=k+1}^{n+1} a_i \pmod 2. \tag{13}$$

The k position reflected digit is found by adding all the digits to the left of the k position of the reflected number to the k position conventional digit, dividing by two and keeping only the remainder. (Refer to Table III).

The equations developed in (9) and (10) may be used directly to translate from conventional binary to reflected binary. This results in:

$$a_k = e_k + A_k \pmod 2, \tag{14}$$

but

$$e_k = A_{k+1} \pmod 2 \tag{15}$$

therefore

$$a_k = (A_k + A_{k+1}) \pmod 2. \tag{16}$$

In words, to find the reflected binary digit in position k add (mod 2) the conventional binary digit in position k to the conventional binary digit in position $(k+1)$.

Applications

As creatures of habit we tend to prefer the decimal system. In performing an analog-to-digital conversion the difficulties noted in the first paragraph of the section on theory are to be reckoned with. To keep the decimal system and at the same time obviate the ambiguities of conversion, the newly developed reflected decimal may be employed. With a series of cams built with twenty rather than ten discrete steps analog information could be converted, without ambiguity, into digital form. By electrical means and using the equations for translation developed here, the reflected decimal information thus obtained could be easily converted into the conventional decimal form.

Thus using cams with ten increasing forward steps and ten decreasing forward steps of uniform amounts cascaded as required, a shaft rotation could be converted unambiguously into reflected decimal form. By use of a small number of relay trees, this could be converted into conventional decimal, maintaining the feature of unambiguousness.

Analog Multipliers and Squarers Using a Multigrid Modulator*

R. L. SYDNOR†, T. R. O'MEARA†, AND J. STRATHMAN†

Summary—**This article describes the use of a multigrid vacuum tube as an AM multigrid modulator multiplier. The accuracy of the multiplier is dependent only upon the linear properties of the vacuum tube used and not upon careful adjustment of the operating potentials. It is unusual that such a simple device should give a range of 78 db with only a ±2 per cent full scale error. The advantages and also restrictions of this device along with a complete range of dynamic performance are included in this article.**

Introduction

THE APPLICATION of the multigrid vacuum tube in multipliers and squarers has been described in the literature [1]; however, these devices have almost always used the dc or static characteristics of the tubes involved. It has also been recognized that a linear modulator or a combination of modulators can be utilized as a multiplier. Although a number of multipliers utilizing the FM-AM principle have been described [15–17], very little literature is available describing the performance obtainable with a simple AM multigrid modulator multiplier [13] (MMM). The usual class C modulator whose output may be quite linear with respect to one input is, obviously, not suitable for multipliers. There are numerous advantages in using a multigrid tube dynamically as a linear modulator [Fig. 1(b)] rather than using the same tube as a static or dc device [Fig. 1(a)]. Probably the most outstanding of these advantages is the elimination of any need to balance out the residual, or dc, electrode potentials. Nonlinear variations in the grid characteristics, which contribute higher powers than the second in a Taylor's series expansion of the tube characteristics, are less detrimental, because most of these high order terms do not contribute to a second harmonic output in the dynamic device.

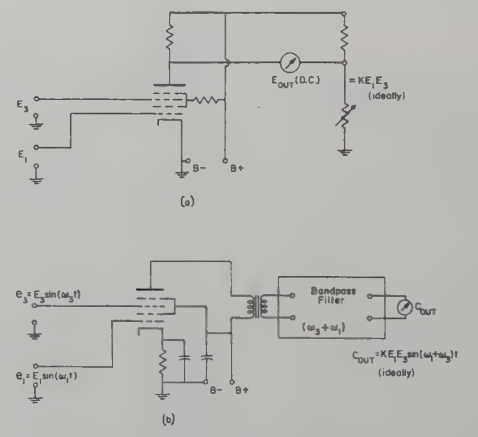

Fig. 1—(a) Static or dc multiplier. (b) Dynamic or modulator multiplier.

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† Electrical Engineering Department, University of Illinois, Urbana, Ill.

Although these differences are sufficiently large to restrict the dynamic range of the dc multigrid multiplier, the dynamic range of the MMM is at least comparable to other more elaborate devices.

It is also important to distinguish between the multigrid modulator or multiplier and a modulator which depends on applying the two signals to a single nonlinear input [11, 12]. The latter usually depends on the square term in its Taylor's series expansion, with filters used to remove all the output components except the one (at ω_0 for example) which is proportional to the product of the two inputs. Almost always such a device will contain higher order terms of appreciable magnitude in its Taylor series representation; about half of these terms may contribute appreciable ω_0 components for strong signal inputs. Because these extraneous terms at ω_0 contribute magnitudes which are proportional to something other than the desired product, an error results from strong signals. In the multigrid modulator, however, the only nonlinear term which is present (ideally) is the cross product term in the Taylor series expansion of two variables (for the plate current I_p in terms of two input or control voltages E_1 and E_3).

It is obvious that any multiplier is also potentially a square law device. It is perhaps not so well known, however, that a combination of square law devices may be arranged as a multiplier by the *quarter square* technique. Similarly, by cascading multipliers, it is possible, in theory at least, to realize any desired integral power expansion with the outputs being at a frequency multiple of the input frequency just equal to the desired exponent.

The fundamental advantage of the MMM square law or higher power device over other nonlinear power law devices is that the accuracy of operation is dependent on only the linear properties of the vacuum tubes and does not require careful adjustment of operating potentials or tube selection in order to realize the desired nonlinear properties. Perhaps it would be more precise to say that operation is dependent on linear characteristic curves, as a square law device must be inherently nonlinear in its operation. The MMM is basically a four quadrant device in the sense that algebraic sign information is preserved in the output. Although the extraction of the sign of the output is not always straightforward, one possible technique to determine it is to square one of the inputs, the reference, and compare the phase of the resultant with that of the multiplier output. More exactly it is a phasor multiplier in the sense that, given two inputs expressible by e_1 and e_3:

$$e_1 = A_1 e^{j(\omega t+\theta_1)} \tag{1}$$

$$e_3 = A_3 e^{j(\omega t+\theta_3)}, \tag{2}$$

the output is (ideally) expressible as e_0:

$$e_0 = KA_1A_3 e^{j(2\omega t+\theta_1+\theta_3)}. \tag{3}$$

It is seen that phase information is preserved in the output.

Multiplier Operation, Circuits, and Data

The diagram of the circuit which was used for multiplier action is shown in Fig. 2. The grid bias was set at a negative seven volts for both grids, the signal sources E_1 and E_2 had accurately calibrated db attenuators which were used to vary the signals independently, and the output was read directly in db on the db scale

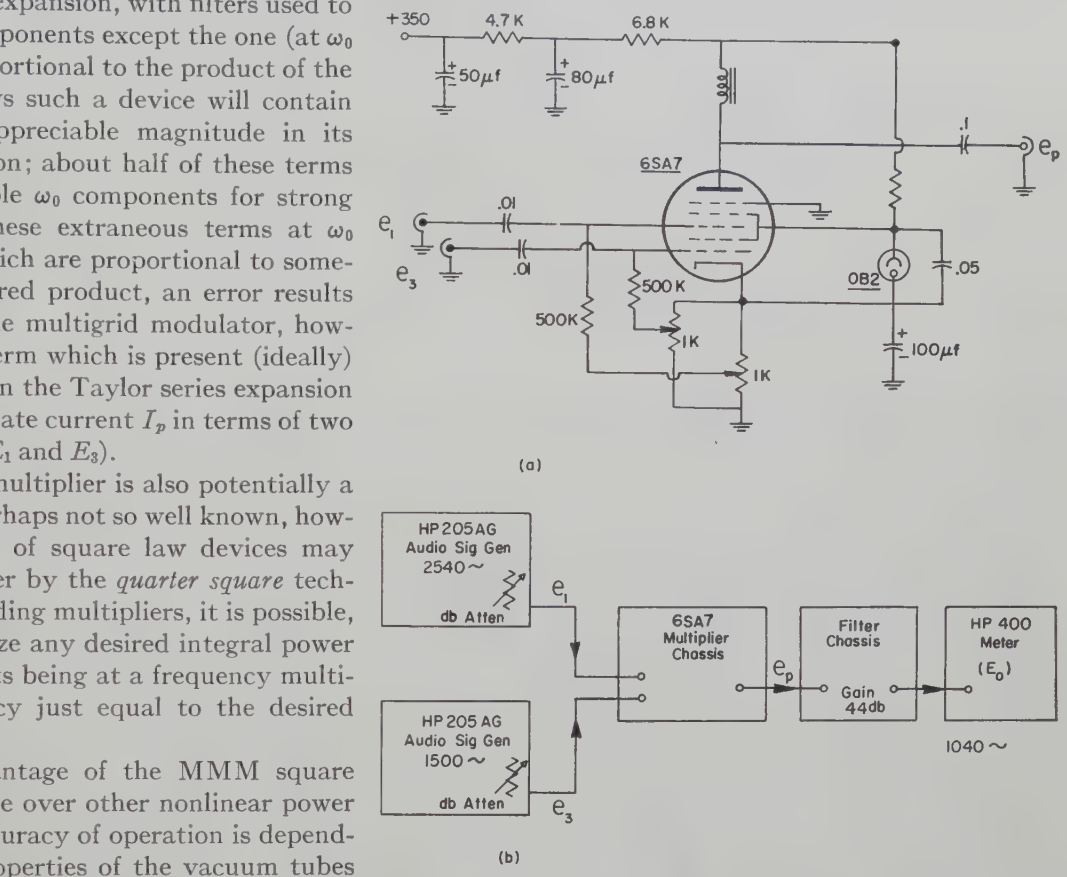

Fig. 2—(a) Circuit diagram of 6SA7 multiplier chassis. (b) Experimental circuit for multiplier data.

of the meter. The data in Fig. 3 was taken by running curves of constant output while varying both input signals. The dotted line in Fig. 3 encloses the region wherein the error in the output was less than one db, whereas the error in the shaded region was nearly equal to one.

The position of the boundary on the low output end of the useable region was determined by the random and microphonic noise from the multiplier tube, the block-band attenuation of the filter, and the sensitivity of the measuring instruments. The position of this boundary in Fig. 3 was determined mostly by random noise and by microphonics in the multiplier tube.

Because many authors have failed to point out that the accuracy of their multipliers was limited at the low end by considerations of noise, balance drift, dc drift, etc., most have not specified an over-all range of dynamic performance. This makes comparison of MMM performance with other types of multipliers difficult,

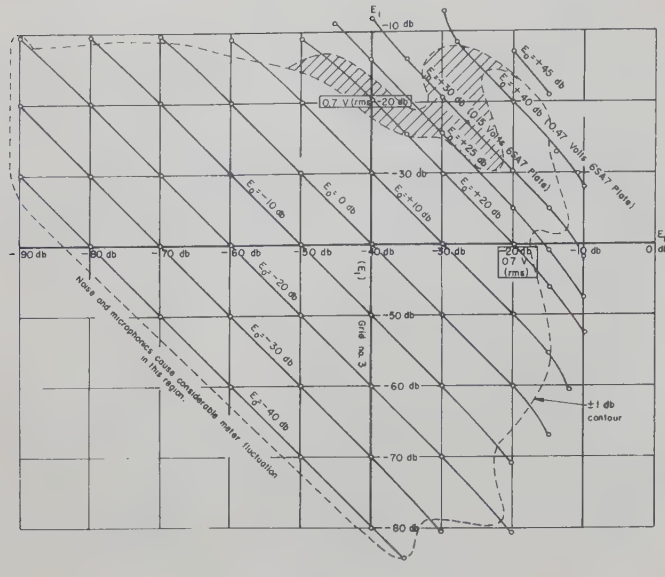

Fig. 3—Multiplier data.

but at least its range appears comparable to more elaborate multipliers. For example, the data given by Mehron and Otto [14] imply a dynamic range of about 60 db with ±1 db precision.

Square Law Operation of the MMM

The circuit and data of Fig. 4 demonstrate the results obtained by using the MMM as a square-law device. Push-pull input was used to minimize error because of even order signal generator harmonics. It will be noticed that it is important to balance the input for minimum output at the plate of the multipliers (point x) rather than at the output of the filter chassis (point y), since the fundamental and signal generator distortion are much larger than the square law second harmonic at the plate of the multiplier, and are easy to balance out. At the output of the filter, however, the only components present are second harmonics, and one is apparently balancing the multiplier second harmonics against the second harmonic distortions from the signal generator, thus obtaining a false null position with the results shown. The potentiometer position corresponding to this adjustment was badly unbalanced; the input signals to the tubes were very unequal.

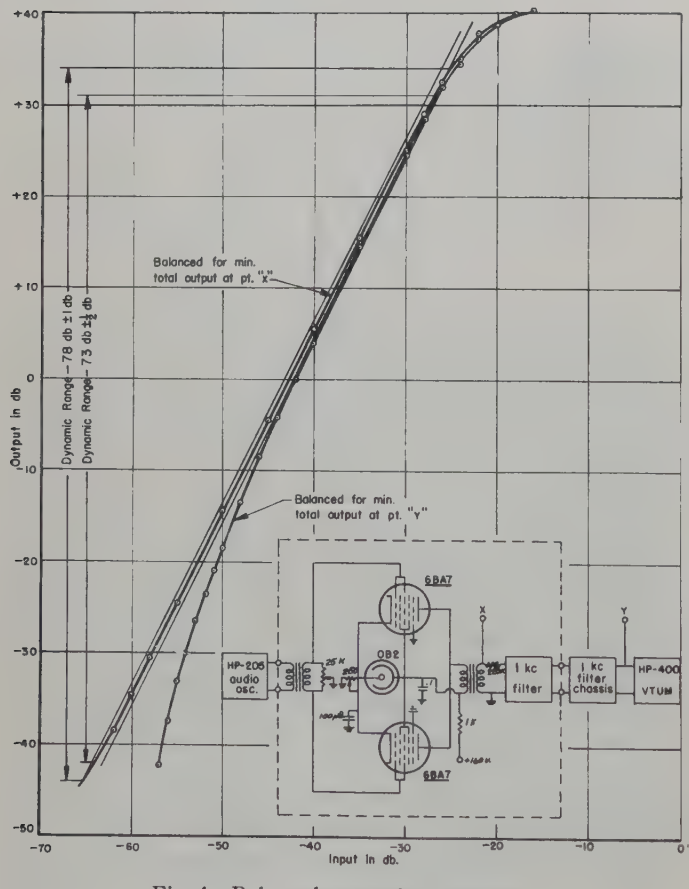

Fig. 4—Balanced square law multiplier.

The accuracy of most other squaring devices has been specified in terms of per cent deviation from *full scale* rather than in terms of dynamic range. The measured *full scale* accuracy (with 15 volts rms taken as full scale) is within ±2 per cent (Fig. 5). This may be compared to about 0.1 per cent for the string of diodes as a parabolic function generator [4] and about 2 per cent for the Raytheon QK-329 beam deflection squaring tube [6].

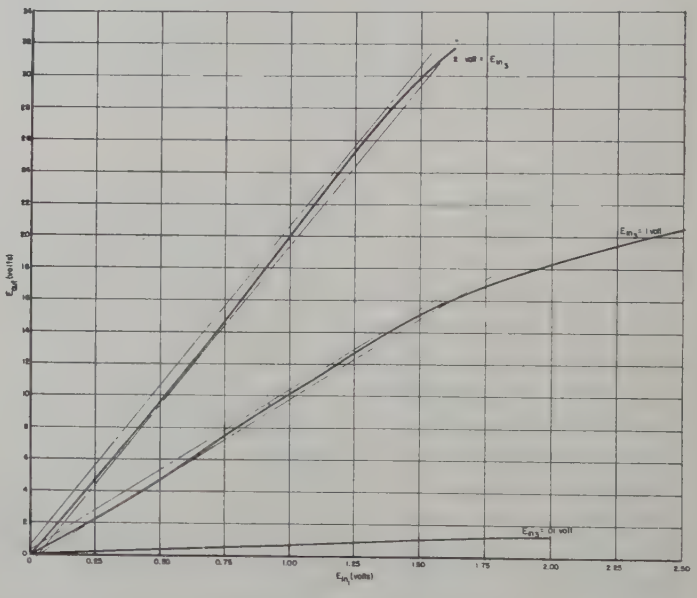

Fig. 5—Linearity curves.

The circuit has a surprisingly good long term stability as is shown in Fig. 6. This test was started with new tubes which explains the early variations in output. However, the output varied less than 0.1 per cent after the initial tube break-in period.

The linearity of a group of twelve randomly selected tubes is shown in Fig. 7. The linearity is within the above stated ±2 per cent full scale value. The constant K in (3) does, however, vary from tube to tube. K is tabulated in Fig. 7 for the group of tubes used.

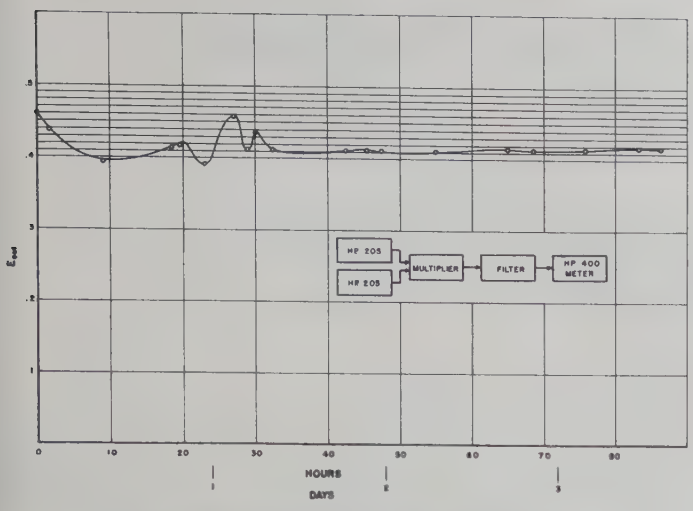

Fig. 6—Long-term stability of multigrid modulator.

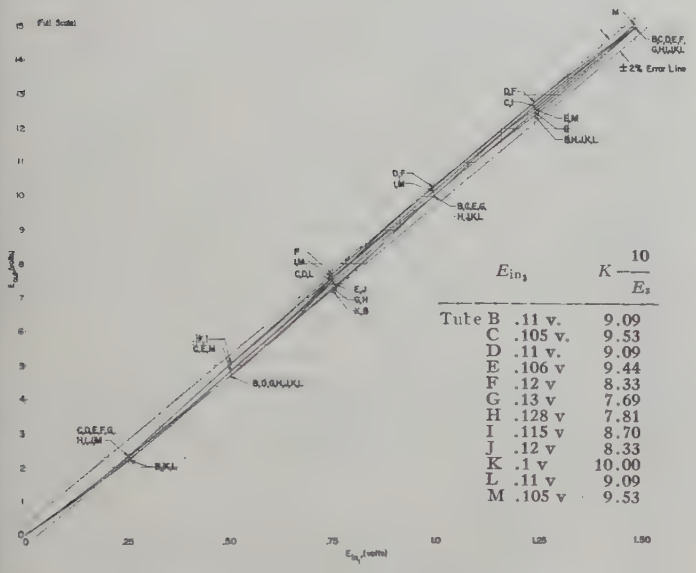

Fig. 7—Linearity curves for 12 randomly selected tubes.

Conclusion

The multigrid modulator multiplier can be used as a reasonably accurate multiplier over a good dynamic range (on the order of 78 db, ± 1 db error or 74 db, $\pm \frac{1}{2}$ db error, as a square law device). It is particularly suitable to applications which take account of its limitations:

1) It basically operates only on ac signals and in many applications it is preferable that these signals be pure sine waves. It is not, however, suited for applications such as multiplier voltmeters wihch require dc multipliers.

2) Its output frequency differs from its input frequency or frequencies (usually it is the second harmonic) unless special provision is made.

3) Its dynamic range is best when it is used as a narrow-band device; (*i.e.*, when the speed of operation is somewhat limited). This is only a noise problem, however, and the analogous situation exists in many multipliers.

4) In its basic form it does not lend itself to inverse feedback techniques to stabilize against tube aging, etc.

The MMM is quite insensitive to tube changes, however, in the sense of these affecting the law of operation (multiplication, square law, etc.). Tube changes affect only the gain constant over the largest part of the dynamic range of operation.

There is need for a multigrid tube designed especially for multiplier work; *i.e.*, one designed so that its grid characteristics are more linear than in existing tubes.

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Transistors in Current-Analog Computing*

BRANCH P. KERFOOT†

This paper was presented at the Western Electronics Show and Convention (WESCON) in San Francisco on August 26, 1955. The paper is published here with only minor changes from the text and figures originally prepared for WESCON presentation.

—*The Editor*

Summary—**A system of electronic analog computing is described in which *current* is used as the variable. The paper indicates that the circuit properties of transistors make them especially suitable for use in operational amplifiers for this computing technique.**

Experimental direct-coupled amplifiers are shown which have been built and evaluated using low-power, low-frequency transistors. The amplifiers have been employed under laboratory conditions to perform the operations of summation, scale-change, integration, and differentiation.

The factors which determine computing accuracy are analyzed, and a new technique of error prediction (based on square-wave output) is discussed.

The paper concludes that the current-analog method promises to use transistors effectively.

FOR THE engineer who is designing and using analog computers, an area of keen interest has been the development and maturity of the transistor as a reliable circuit element. Now that the junction transistor has gained the recognition of military approval and has become available in quantity, some of its properties, such as reliability and physical advantages, offer promise for computing applications. Both the analog computer and the transistor are moving out of the laboratory and into industry on expanding scales. It will be the purpose of this paper to discuss one method by which they can join forces, and to cite experimental results which indicate some of the resulting potentialities. Under laboratory conditions, and using the current-analog method, present transistors *can* replace vacuum tubes in many modern electronic analog computing applications. Further transistor developments promise even better analog computers in the future.

The advantages of using transistors in any analog computer are numerous. Their use, along with other recent subminiature components, permits relatively complex electronic equipment to be compacted into small space and to have reasonable power consumption. A pack of ordinary playing cards has a volume comparable to approximately three times that of the simple operational amplifiers to be described.

The impedance properties of transistors bear a close resemblance to the admittance properties of vacuum tubes in the normal, gainful connections. It is natural then to consider the transistor as operating upon currents, much as we are used to considering the triode vacuum tube handling voltage signals.

An individual transistor often has low input impedance and high output impedance. An amplifier formed by cascading such stages will also have low input and high output impedances. These properties are ideally suited to handling a current as the signal-carrying variable.

Several outlines of the possibility of using the current-analog principle have appeared in the literature. These include Shea's book[1] and Hellerman's article.[2]

Each of the figures which follows serves to take the place of lengthy descriptive text, for each shows an aspect of the study of current-analog computing.

Table I lists the more important pros and cons of using present-day transistors (at least those available on the market) in electronic analog computers.

TABLE I

PROS AND CONS OF TRANSISTORS AS CIRCUIT ELEMENTS IN AN ANALOG COMPUTER

Advantages	Disadvantages
Size is smaller than vacum tubes.	Price is relatively high.*
Power consumption is low.	Temperature sensitivity is significant.*
Rugged physical packaging is inherent.	Frequency response is inferior to vacuum tubes.*
Life expectancy is relative long.	Large signal capabilities are inferior.*
Drifts in dc circuits are controllable.	Power gain per stage is somewhat lower.

* Expected to be overcome in the near future.

The important feature to note about this table is the *ultimate* situation which will occur when the disadvantages which are listed have been removed. It is this bright

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[1] R. F. Shea, "Principles of Transistor Circuits," John Wiley and Sons, New York, N. Y., pp. 413–421; 1953.

[2] H. Hellerman, "Some transistor building blocks for analog computers," *Communications and Electronics* (*AIEE*), No. 14, pp. 410–413; September, 1954.

prospective unbalance toward the left which makes one anxious to get started in applying transistors for this use.

Examples of the advantages are:

1) Transistor size is commonly less than 1/40th of the volume of a miniature vacuum tube.
2) Transistor power consumption is typically 1/60th of the total quiescent power of a miniature tube.
3) Transistors can be thrown on a concrete floor without breakage.

Recent studies (to be published) of the life expectancy for transistors have been made by RCA-Camden. The results indicate that early estimates of transistor life in proper use of 70 thousand hours were conservative. This figure should be compared to the one to three thousand hours of life expected for a premium vacuum tube.

Junction-transistor drift of dc biases, for an individual transistor, obeys well-defined laws, such as the dependence on temperature.[3] One major source of bias fluctuation in a transistor circuit can thus, by due care, be controlled more easily than, for example, contact potential variations in a vacuum tube.

Progress in transistor design since the date of the experimental work here has already overcome at least two of the disadvantages listed in Table I. Transistor frequency response now extends well into the megacycle region,[4] and the large-signal capabilities, in the power-handling sense, have reached an order of several watts and more.[5]

The work of several others, such as Blecher of the Bell Telephone Laboratories[6] and Ettinger,[7] has been directed toward transistorizing operational amplifiers to be used in the conventional voltage-analog computing manner. Their results indicate that comparable accuracies could be obtained by both methods for transistors available at the times.

This paper summarizes the results of attempts to capitalize on the advantages of transistors which were listed above. By means of employing a revised computing system the circuits can be tailored to make best use of the fundamental transistor properties.

A concise picture of the analog principles on which current-analog computing operates is obtained by a direct comparison with the existing methods of voltage-analog computing. For this reason the next figures show a side-by-side presentation of current computing in terms of the well-developed and familiar voltage-computing practices.

[3] Shea, *op. cit.*, pp. 45–49.
[4] W. E. Bradley, *et al.*, "The surface barrier transistor," PROC. IRE, vol. 41, pp. 1702–1720; December, 1953.
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Current-Computing Fundamentals

The basic building blocks of analog computers are the operational units which perform specific mathematical operations upon the variables.

Fig. 1 illustrates the interconnection of two precision passive circuit elements with an electronic operational amplifier (the triangular block) to perform the computing operations described. The circuit arrangement of elements is shown as it is commonly used for voltage-analog computing, along with the corresponding arrangement when current is the variable. One notes that similar elements are used in both cases.

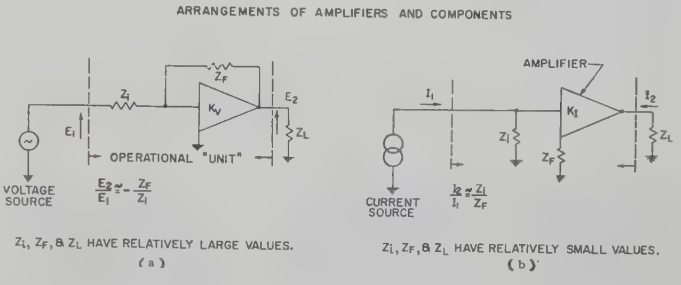

Fig. 1—Isolation and multiplication by a constant. (a) Voltage analog computing: Z_i = "summing" impedance, Z_f = "feedback" impedance. (b) Current analog computing: Z_i = "summing" impedance, Z_f = "feedback" impedance.

Behavior of the current-computing unit in the operation of isolation may be described briefly as follows. In the right hand portion of Fig. 1, the high-gain current amplifier, K_I, receives a small part of the input current, namely the part which is not shunted to ground by the low impedance Z_i. The small signal current is amplified linearly and reversed in polarity. The amplifier's output current, now much larger, passes through both the load and through Z_f. As it passes through Z_f it raises or lowers the voltage at the upper end of Z_f in phase with the voltage signal across Z_i due to the input. The input signal to the amplifier itself is thus greatly reduced from what it would be if this Z_f were zero impedance, and the resulting high degree of degenerative feedback has several beneficial effects. First, the feedback reduces the shunting effect of the amplifier across the precision Z_i so that the input impedance of the over-all unit is accurately known. Second, the feedback effectively magnifies the output impedance of this over-all unit very greatly, so that the unit appears to the succeeding one or more stages as an excellent current source of very high impedance. These are the desired properties of an isolation unit for current computing.

In the two diagrams of Fig. 1 it is important to note the relative positions of the precision summing impedance Z_i and the precision feedback impedance Z_f. The position of this Z_f for current computing reminds us of the feedback present in a cathode-follower circuit.

Analytic relationships, which are suitable for most purposes, for the transfer of signal from input to output of these computing units may be derived with the aid of Fig. 1. For voltage-computing

$$\frac{E_2}{E_1} = \frac{Z_f K_v}{Z_f + Z_i(1 - K_v)},$$

where K_v is the open-loop voltage gain of the amplifier alone. The comparable relation for current-computing is

$$\frac{I_2}{I_1} = -\frac{Z_i K_I}{Z_i + Z_f(1 - K_I)},$$

for the signal polarities shown. K_I is the current gain of the basic amplifier when the feedback loop is removed and the amplifier drives a similar load impedance.

The accuracy of computation may be determined to a large degree by how closely the two gains, K_V and K_I, approach infinite magnitudes. As those conditions are approached, the transfer ratios become in both cases simple ratios of precision passive impedance elements as shown in Fig. 1.

How Can Current-Computing Be Applied?

The next few figures show how the current-computing method is applied to familiar voltage-computing tasks.

Fig. 2 shows the idealized addition operation. Each term in the outputs of both methods is the familiar ratio of impedances multiplied by input signal. Typical values might be: 1) For voltage computing, Z_f of one megohm and Z_i's of one-tenth to one megohm. 2) For current computing, Z_f of one hundred ohms and Z_i's of one hundred to one thousand ohms.

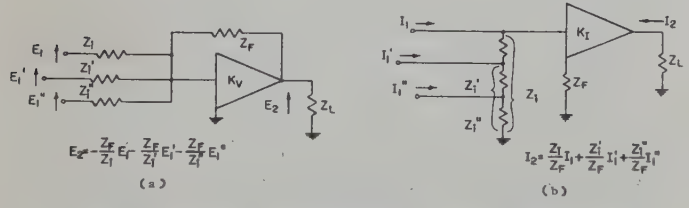

Fig. 2—Operation of summation. (a) Voltage computing. (b) Current computing.

Fig. 3 shows a calculus operation and a choice of methods. The lower case letters refer to time variables where no initial conditions have been included. In the uses shown the amplifiers serve to buffer output from input and to allow long time constants without prohibitive attenuations.

The techniques developed in voltage-analog computing to select time scales and impedance values are all of great value in making similar choices for current computing. The current-variable system is indebted to the principles of voltage computing for most of its basic lore.

Fig. 4 presents corresponding methods of differentiating. Such an operation is used in fire-control radars to calculate the rate of change of, for example, a coordinate variable to develop a velocity variable.

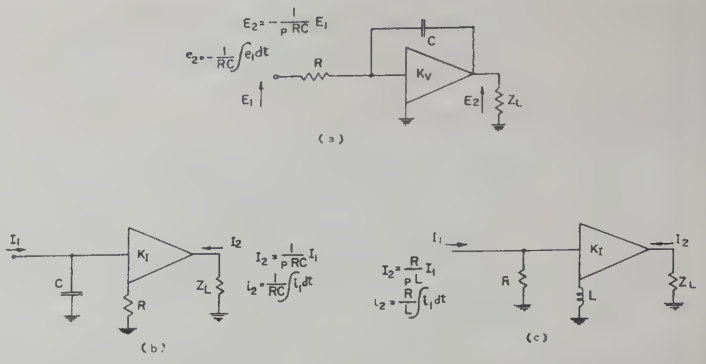

Fig. 3—Methods of performing integration. (a) Conventional voltage computing. (b) Current computing with C and R. (c) Current computing with R and L.

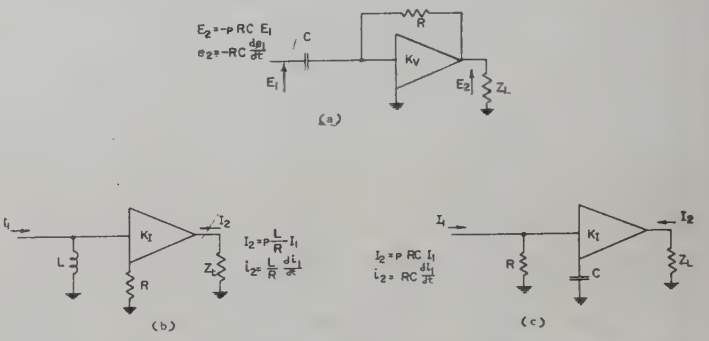

Fig. 4—Methods of performing differentiation. (a) Conventional voltage computing. (b) Current computing with L and R. (c) Current computing with R and C.

How Has Current-Computing Been Demonstrated?

Fig. 5 and the four following figures show some qualitative test results. The four voltage waveforms were photographed from an oscilloscope located at the points shown, and from these voltages the currents which flow in the various leads may be inferred.

Fig. 5 shows a simple typical operation, the addition of a sine wave and a square wave to yield the expected composite output signal. The forward current gain, K_I, of the transistor amplifier used here was approximately 1,000. An over-all current gain of 10 will also be noted, measured from the two generators to the load.

Fig. 6 illustrates the resistance-capacitance method of integrating. Here a square wave is converted into a triangular form. One notes that the amplifier with its resistive feedback, R_f, acts to sample the voltage across the capacitor, and to develop a large output current which is proportional to it.

Fig. 7 shows the other arrangement of elements for integration. The imperfect inductor used, which had appreciable series resistance, caused imperfect integration, as evidenced by the curvature of the output triangular waveshape.

Integration with R and C did not have this curvature, so that the importance of using a low power-factor reactive element is emphasized. An engineering decision, as to which method of integration to use, can be based on

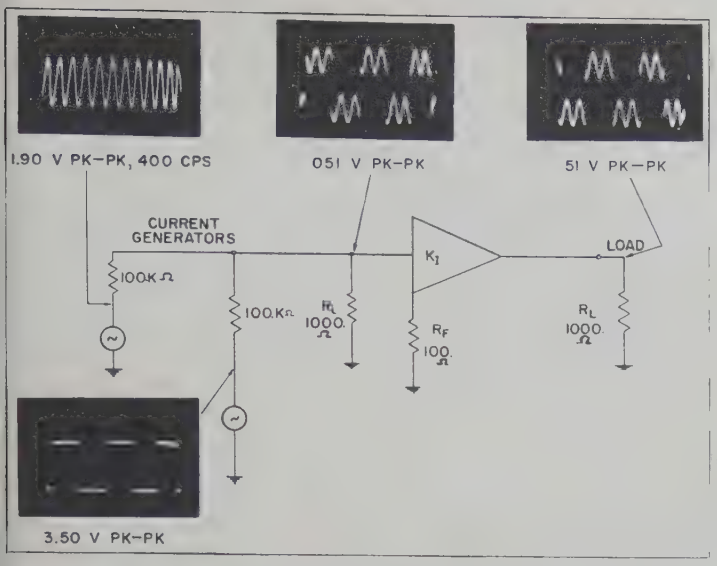

Fig. 5—Example of summing and scale change. Voltage waveforms shown.

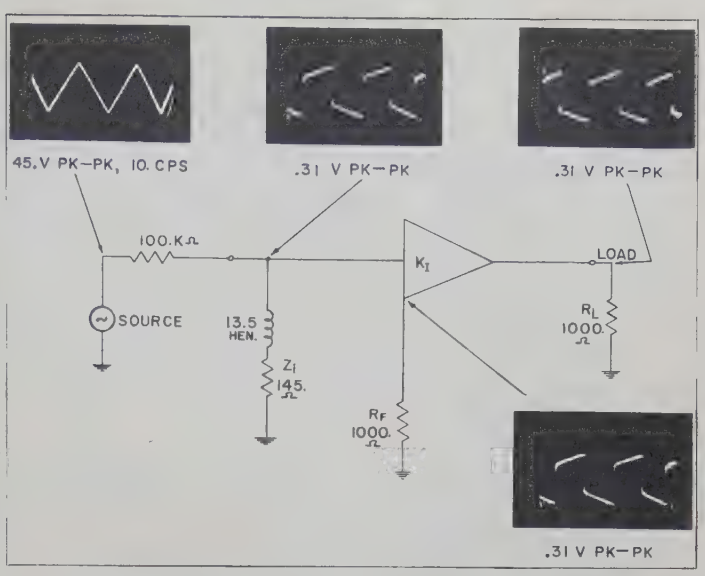

Fig. 8—Example of R and L differentiation. Voltage waveforms shown.

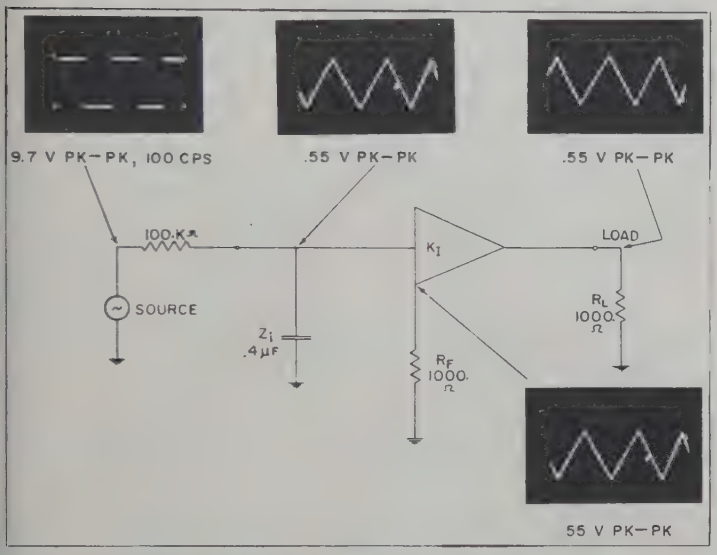

Fig. 6—Example of R and C integration. Voltage waveforms shown.

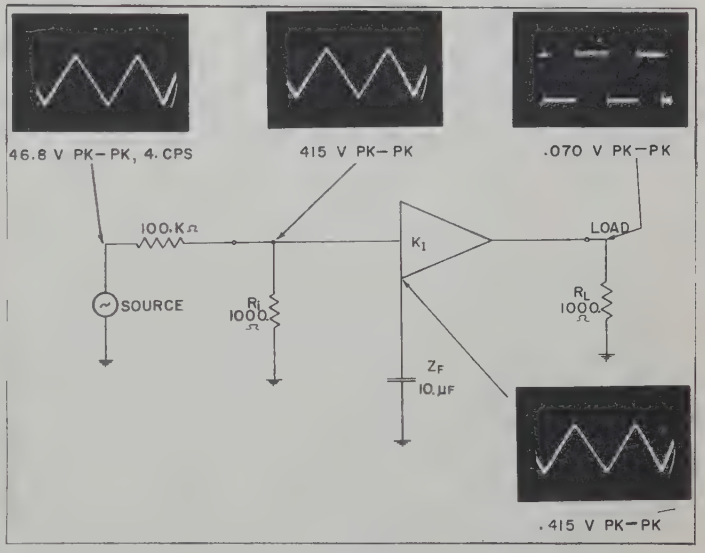

Fig. 9—Example of R and C differentiation. Voltage waveforms shown.

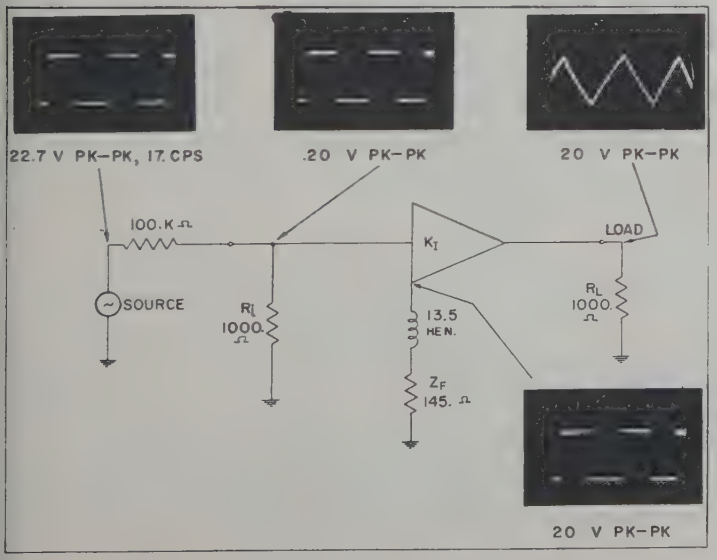

Fig. 7—Example of R and L integration. Voltage waveforms shown.

impedance level, on the reactors available, and on the time scales needed.

Fig. 8 demonstrates differentiation. Again an imperfect inductor causes the output signal not to be the desired signal. The net output is a combination of square wave and the triangular wave which effectively leaked through after appearing across the resistive 145 ohms of Z_i.

The amplifier with resistive feedback through R_f is sampling the whole voltage across the inductor and is developing an output current of like shape.

In Fig. 9 more accurate differentiation occurs using a resistor and a capacitor. One notes some oscillation or ringing at the output leading edges. This particular amplifier did not have sufficient phase control to be used in the differentiation operation. Rate of decay of the ringing is a measure of circuit stability in this connection.

What Sort of an Amplifier Does Current-Computing Require?

The list of Table II includes the desirable new features which an operational amplifier for current-computing should have. In addition, one designs the amplifier to have the customary properties of low noise, adequate bandwidth, interchangeability of transistors, and sufficient power output capabilities.

TABLE II

Basic Open-Loop Amplifier Properties to Be Emphasized for Current Computing

a) High current gain.
b) Low input resistance.
c) High output resistance.
d) Controlled gain and phase responses to permit closing the feedback loop with stability. Maximum open-loop phase shifts are:
   180° for summation or isolation
   90° for differentiation
   270° for integration
e) Packaging for isolation from ground to permit a "floating" amplifier.
f) Compensation for dc offset caused by temperature variation.

The Nyquist condition for an unconditionally stable closed loop involves the design of a basic amplifier whose gain and phase responses are broadly as listed in item *D* of Table II. For low frequencies of operation the dc amplifier itself has a net phase reversal from input terminal to output. As frequency increases most amplifiers acquire lagging phase angle which is added to the basic phase reversal. At some high frequency this phase lag alone will reach 180 degrees. If the input and feedback impedances, Z_i and Z_f, do not contribute additional phase shift, as, for example, in the operation of summation, then the portion of the output signal which they return to the input will also be 180 degrees lagging. A condition for oscillation exists if the portion of the net output signal, as modified by the input and feedback elements, which reaches the input terminal is in phase with an equal to or larger than the signal already present at the amplifier input. Such will be the case, for summation, at the frequency where the amplifier phase lag reaches 180 degrees from the low-frequency phase relationship.

For differentiation, the input and feedback impedances are chosen deliberately to introduce close to 90 degrees of phase lag for the feedback signal in the frequency range of the computing variables. This is a necessary choice to differentiate. In order to prevent the regeneration just mentioned, which resulted from a net of 180 degrees of phase lag in the amplifier combined with Z_i and Z_f, it is required that the amplifier itself be designed to have at high frequencies less than 90 degrees of phase lag (in addition to its normal low-frequency phase reversal).

Similarly, since integration involves a choice of Z_i and Z_f which adds nearly 90 degrees of phase lead to the returned signal, the basic amplifier may be designed to allow up to 270 degrees of internal phase lag at some frequencies, before the danger of oscillation exists. In this case the feedback elements may liberalize the amplifier's design requirements before a net phase lag of 180 degrees is reached back at the input to the amplifier.

As engineers well know, it is always good practice to allow suitably wide safety factors for phase margins from the limits which are stated in item D of Table II.

The requirement stated in item *E* implies one or more floating power supplies to energize the active elements in the amplifier. Several techniques offer promise for delivering the bias power with isolation from ground which is adequate for a given accuracy goal.

1) When the feedback element, Z_f, is resistive or inductive a common, grounded power supply can be used, with Z_f acting as return dc path. The actual power input to the amplifier would come from an equivalent high-impedance current source in the supply, where the impedance is made too high to shunt the precision element appreciably.

2) When the feedback element is capacitive the power can be transmitted to the computing amplifier on a high-frequency carrier from a common source using the same path as in 1), or possibly using air-core transformer coupling. The carrier is rectified and filtered by simple elements which float with the amplifier. The carrier frequency chosen is somewhat above the highest signal frequency of interest in the analog variable.

3) Another method of using a common, grounded power supply might involve a pair of output terminals for each amplifier where *both* leads are electronically isolated from ground by current regulators.

In summary of Table II, the low input and high output impedances are the most significant innovations of current-analog computing.

Properties of the Operational Unit

When the operational amplifier is combined with precision impedances to form an operational unit, the unit may then be considered as a *black box*.

Fig. 10 shows the appearance of the operational unit as viewed by source and by load. One notes in particular the low input impedance and the high effective output impedance (which involves a factor times the current gain of the amplifier).

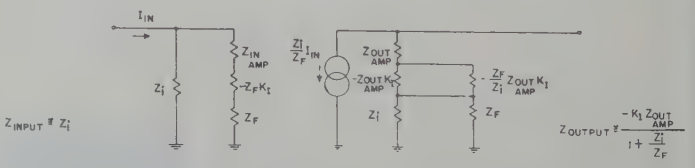

Fig. 10—Equivalent circuit of closed-loop unit, where Z_i is precision summing impedance; Z_f is precision feedback impedance; $-K_1$ is amplifier open-loop current gain; Z_{amp}^{in} is input impedance of basic amplifier; Z_{amp}^{out} is output impedance of basic amplifier; $(Z_i/Z_f)I_{in}$ is equivalent current generator.

How Can Computing Accuracy Be Simply Expressed?

A universal analytical method of error determination is desired for all of the computing operations which have been mentioned.

Fig. 11 illustrates the method suggested. The error is measured as the closeness to an ideal step *output* waveform which the actual output from each of the operations achieves. Only one operational unit is considered at a time. Note that different input signals are required for each operation to produce the step output. An analytic relation can be developed (usually based on the circuit of Fig. 1 and on the equivalent circuit of Fig. 10) for the actual, imperfect transfer of signal through the operational unit which results in the dotted outputs. For laboratory tests, the ideal input waveforms are easily generated, sufficiently accurately, by conventional sources of wide-bandwidth signals.

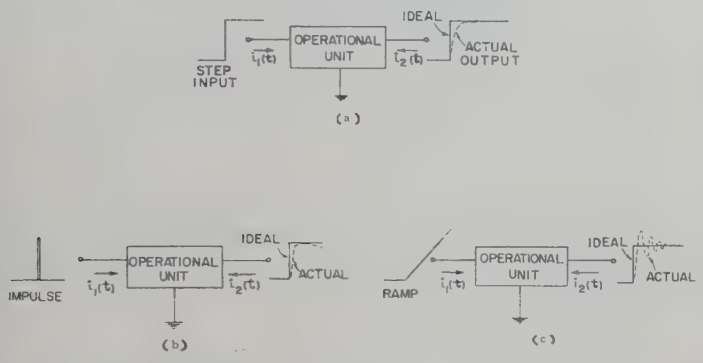

Fig. 11—Waveforms considered in error analysis. (a) Operation of isolation. (b) Integration. (c) Differentiation.

Fig. 12 shows, in the same relative positions as Fig. 11, the calculated errors which occur because the actual outputs are not really the desired step waveforms. These errors are the instantaneous differences between actual outputs and steps having corresponding scale factors. In order to calculate these error values certain properties of the amplifier were measured and then used in the expression for transfer function which is derived from the equivalent circuit and the connection of computing impedances. The measured properties were gain-vs-frequency response and the impedances which appear in the equivalent circuit of the amplifier alone. The accuracy of the resulting calculations depends directly on how well the true equivalent circuit is known. Since the passive computing elements used in these calculations differ from the ones used for the earlier photographs, there is not direct numerical correspondence between those photographs and the calculated errors. The calculations cited serve to illustrate the method of analysis which has proven useful.

The oscillations of the error, which are indicated for the case of differentiation, come about through the measured gain-phase responses. If the oscillations had not shown up analytically, there would be an obvious discrepancy between observed and calculated results. The operation of differentiation can be performed with this amplifier with suitable accuracy, if the oscillations decay sufficiently rapidly in our time scale of interest.

The errors shown in Fig. 12 are instantaneous values, and as such have restricted meaning in the over-all observation of a computing result. In order to present a single measure of error for the computing period, that is, for the time interval over which the solution is observed, one can use a simple rms averaging procedure.

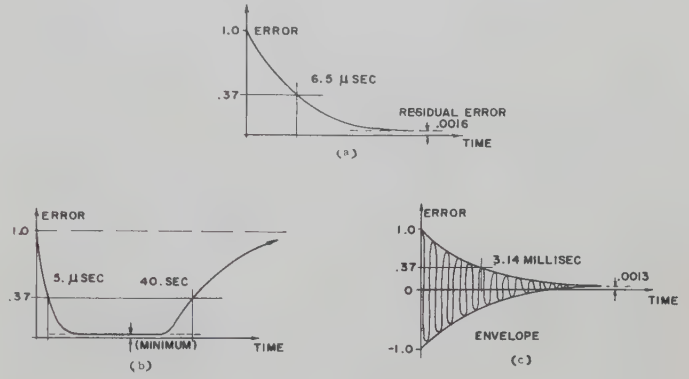

Fig. 12—Instantaneous fractional errors with calculated numerical values. (a) Isolation operation. (b) Integration. (c) Differentiation.

Fig. 13 presents the net rms error for a period of computation, plotted with the length of that period, or interval, as independent parameter. The interval itself is determined by the time scale used in computing. For the particular amplifier and impedances used in the tests and calculations here, it is observed that rms fractional error is less than one per cent for some choice of time scale. For the isolation and differentiation operations the error becomes even less with long computing times.

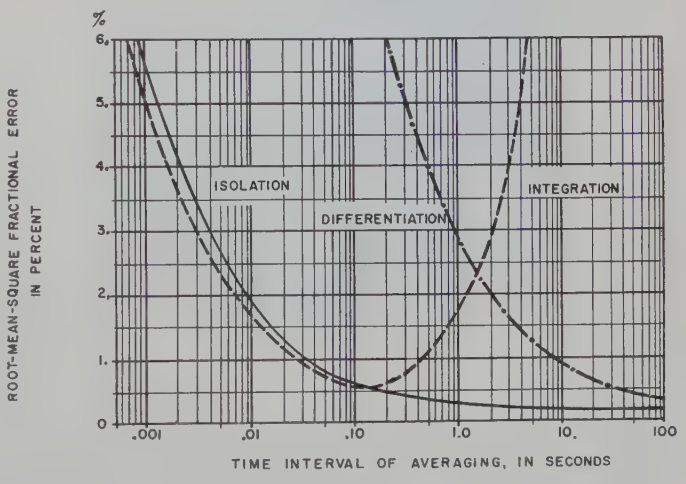

Fig. 13—Calculated rms fractional error for each operation using measured amplifier values.

Curves such as those shown in Fig. 13 can be of great practical value for equipment design or for optimum use of existing equipment. In design, the impedance values and the required amplifier gain can be determined by working backwards from the rms error curves to the analytic transfer relation and then to the needed equivalent circuit properties of the amplifier itself. For utilizing existing equipment, the forward process is employed. The known analytic transfer relation of the unit is used to plot rms error curves like those in Fig. 13. The computing time scale is selected for minimum error.

Where other than step output waveforms are involved, and the linear elements mentioned here are used, the actual output which is expected may be reduced to a series of delayed steps to give an indication of instantaneous error and then of rms error for true waveform.

This technique of rms error appraisal may be applied to voltage-analog computing in the identical manner as has been illustrated here for current computing.

Just What Amplifiers Were Used in These Tests?

Examples of the experimental amplifiers built in the course of this study are shown in the photographs of Figs. 14 and 15. These pictures show two models of the three-stage direct-coupled transistor circuit which was used as the operational amplifier for the qualitative tests which are discussed. The amplifier has been stabilized by phase-control networks for the application of approximately 60 decibels of feedback.

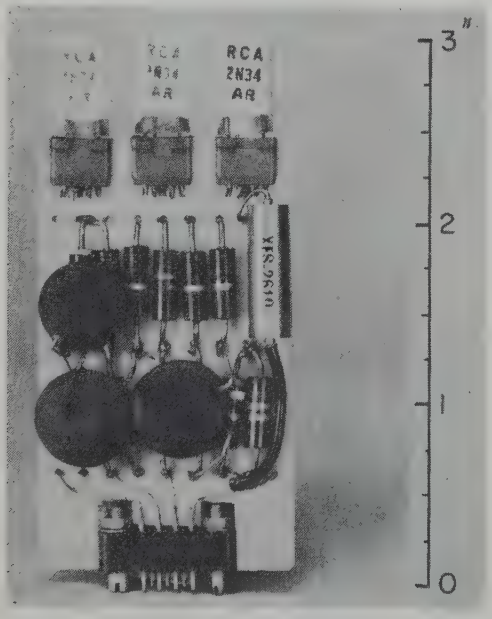

Fig. 14—Transistor current amplifier, card model.

Fig. 14 shows that the layout may easily be adapted for printed circuit and dip-soldering techniques of manufacture. The unseen third dimension of this model is 5/16 of an inch, so that the relatively small over-all volume of $1\frac{1}{2}$ cubic inches is required.

Fig. 15 shows another model of the same circuit. This one has been potted in clear resin to protect the circuit elements from moisture and shock; it is quite rugged.

In any final application, a large number of identical amplifiers will probably be required. Space and power can be used efficiently, so that the amplifiers can be individually withdrawn for test, each as a unit with its own transistors. A simple test jig can be provided to measure the performance of one amplifier at a time.

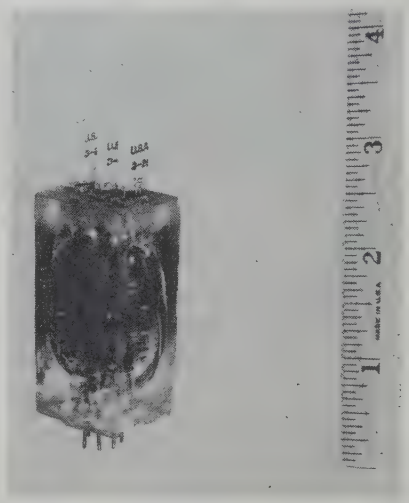

Fig. 15—Transistor current amplifier, encapsulated model.

The schematic diagram in Fig. 16 describes the transistor amplifier which was suitable for these tests. It was built in late 1953 using the type 2N34 transistor available at the time.

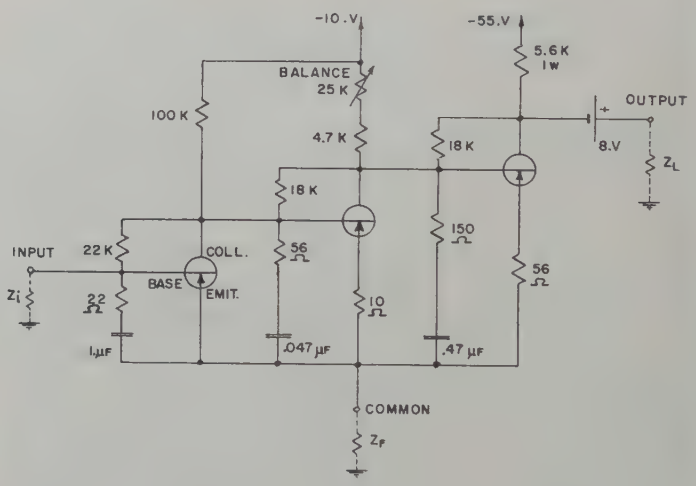

Fig. 16—Transistor current amplifier tested.

The recent availability of improved transistors means that an amplifier designed today would take advantage of greatly improved frequency response, transistor uniformity, and power-output capabilities.

The amplifier is seen to be a three-terminal device which corresponds to the triangular block shown in earlier diagrams. The relative locations of the passive computing impedances and of the load are indicated.

Three common-emitter transistor stages provide the necessary phase reversal. The collector, base, and emitter symbols are marked on the first stage. A balance potentiometer removes any initial offset. Some internal

feedback has been used within each stage to overcome variations between the individual transistor samples.

In this particular circuit, 85 per cent of the total dc power dissipation occurs in the 5.6 kilohm dropping resistor of the third stage. A transistor current-regulator stage could replace this resistor and lower the supply-voltage requirement. Complementary symmetry circuits at the output using *p-n-p* and *n-p-n* transistors, would offer advantages.[8]

How Is Closed-Loop Stability Assured?

Three RC phase-control networks are used to shape the frequency responses to assure closed-loop stability for the isolation and integration operations. Fig. 17 shows the net resulting gain and phase responses of the amplifier alone without feedback elements.

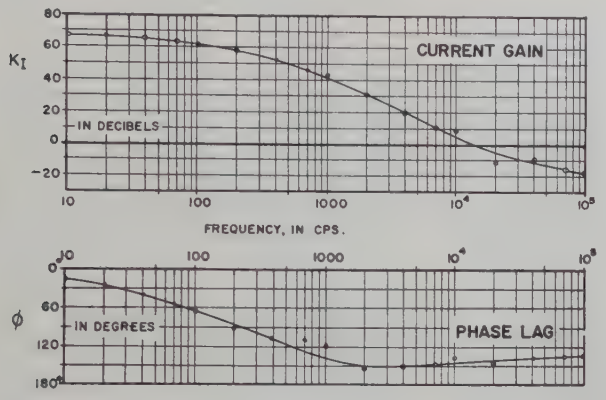

Fig. 17—Measured open-loop responses of current amplifier.

We noted in Table II that the maximum allowable phase lag, at any frequency where amplifier gain exceeds unity, can be up to 90 degrees for stable performance of the differentiation operation. Fig. 17 shows a phase lag of up to 142 degrees, so that we can expect any demonstration of differentiation using this amplifier to show instability at the higher frequencies. The photograph in Fig. 9 illustrates such instability. Since the maximum phase shifts allowable for the isolation or integration operations are 180 and 270 degrees of lag respectively, the amplifier shown here will perform these tasks satisfactorily.

The frequency response of the transistors alone is, of course, much better than the over-all gain response here indicates. The frequency response has been sacrificed to maintain phase control. This situation points out, however, that since transistors of higher intrinsic frequency have become available, it is now possible to build phase-controlled transistor amplifiers which in turn have considerably wider gain responses than shown.

In terms of closed-loop operation, the net phase shift for this amplifier is 0.59 degree or approximately 1/100 of a radian at 400 cycles per second, for the operation of resistive summation. This figure may be improved directly with the gain-bandwidth product of the individual transistors used.

[8] G. C. Sziklai, "Symmetrical properties of transistors and their applications," Proc. IRE vol. 41, pp. 717–724; June, 1953.

Summary of the Properties of the Transistor Amplifier

Table III outlines the properties of the amplifier tested which are important for its application in the current-computing configuration. Numerical values of any current amplifier which one might build for a specific application would naturally reflect the impedances and frequencies which that job needs.

TABLE III
Technical Specifications for Experimental Transistor DC Amplifier

Schematic diagram in Fig. 16	
Open-loop gain and phase responses in Fig. 17	
Number of transistors	3
Type transistors	Low power, low frequency, p-n-p, diffused-junction, such as type 2N34
Open-loop properties:	
Current gain, K_I	−2360
Gain down 3 decibels	65 cps.
Phase angle at unity gain	142°
Frequency of phase reversal	>100 kc.
Input resistance	Approximately 2,500 ohms
Supply power input	460 milliwatts
Normal range of load resistances	100 to 2,000 ohms
Normal maximum current output	±1.4 milliamps

This amplifier has been used under laboratory conditions only. The low power, low frequency transistors were of the alloyed-junction type, and equal performance can be expected with other similar transistors. The drift (for short-circuited output) reached a peak of one-half microampere at the input in a period of three hours. Although not deemed necessary as yet, chopper stabilizing of dc drift using the principles of Goldberg's method[9] has been tried and can be used effectively with current-computing operational amplifiers, for example, to reduce temperature sensitivity due to the transistors.

Conclusion

1) Present transistors can be used quite satisfactorily to build a current amplifier for the current-analog computing method. Experimental dc amplifiers having the desired low-input and high-output impedances have been tested. Transistor operational amplifiers lend themselves to modular-construction techniques.

2) Current computing has been demonstrated qualitatively as a practical technique for performing analog-computing operations.

3) The accuracy of an analog-computing unit can be effectively expressed in terms of an rms measure of its capability to deliver a step output faithfully. This expression of accuracy is helpful in the design, development, and use of an analog computer.

4) Present and future transistor improvements in bandwidth and power handling will be applicable to the widening usefulness of analog computers and of the current-analog method. This method seems to use the peculiar properties of transistors to good advantage.

[9] E. A. Goldberg, "Stabilization of wide-band direct-current amplifiers for zero and gain," *RCA Rev.*, vol. 11, pp. 296–300; June, 1950.

Correspondence

Working Time in Repetitive Analog Computers

In a real time analog computer the product RC in the integrator equals 1 second. The maximum working time t_1 is determined by the requirements of the problem to be solved. t_1 together with the required accuracy determine the gain of the operational amplifier G.

In repetitive analog computers the gain G is limited by economic considerations. Optimum values of t_1 and RC must then be determined. It is the purpose of this note to show a practical way of doing this.

The period T in a repetitive analog computer consists of the working time t_1 and the recovery time t_2. The requirements on t_2 are not very stringent. It should be long enough to permit recovery of the computing units. On the other hand it should not be so large that appreciable computer time is lost.

The choice of t_1 is based on the following considerations. For a unit step input, the output of the integrator has the form[1]

$$e_0 = -\frac{1}{RC}\cdot\frac{G}{G+1}\left[t - \frac{t^2}{2(G+1)RC} + \cdots\right]. \quad (1)$$

Hence if the maximum error is to be smaller than δ per cent

$$t_1/RC \leqq G/50 \quad (2)$$

must hold. The same quotient t_1/RC also determines the extent to which an eventual internal drift in the integrator will spoil the accuracy, and hence it should be kept as small as possible. On the other hand, with low values of t_1/RC the outputs of the integrators are small and high amplifications are required when a problem is set up on the computer. The highest value of t_1/RC permitted by (2); *i.e.*,

$$t_1/RC = \delta G/50 \quad (3)$$

will therefore be chosen here.

Another requirement is one of convenience in reading the output in the case of oscillatory solutions. It is required that something like five full periods should be seen on the cathode ray tube. This may be written in the form

$$f_0 t_1 = 5 \quad (4)$$

where f_0 is the frequency of the solution as it actually exists in the computer ($f_0 = a_t f$ where a_t denotes the time scale and f the true frequency of the solution).

The final requirement arises because of the limit on the accuracy which is set by the bandwidth of the computing units. Errors due to these causes may appear in various forms. MacNee[2] has shown that in the case of the harmonic equation for instance the solution given by the computer may have the form

$$y = e^{[(-2\pi f_0)^2(T_1+T_2/2)-1/T_0]t_1}\cos 2\pi f_0 t \quad (5)$$

instead of $y = \cos 2\pi f_0 t$. T_1 and T_2 denote the high frequency time constants of the adder and integrator respectively and $T_0 = GRC$ is the low frequency time constant of the integrator. It is seen from (5) that if

$$[(2\pi f_0)^2(T_1 + T_2/2) - 1/T_0]\cdot t_1 = 0 \quad (6)$$

the error in question will be eliminated. If in addition both $(T_1+T_2/2)$ and $1/T_0$ are made small separately, the errors will be smaller also in other problems where these quantities appear in different combinations. Further, deviations from f_0 will not strongly affect the accuracy.

Errors appearing in the solution of differential equations containing relay type nonlinearities are at present being investigated. It has already been established that fulfillment of the above requirements will minimize errors due to bandwidth limitations in this type of equation as well.

From (3), (4), and (6),

$$f_0 = \delta 10^{-4}/(T_1 + T_2/2) \text{ cps} \quad (7)$$

t_1 and RC may then be computed by (3) and (4). The value of $T = t_1 + t_2$ arrived at will probably require a high persistency cathode ray tube to obtain a continuous trace. In a suitably designed computer T will be low enough to permit the solutions to follow without appreciable delay changes in the parameters of a problem. This is particularly important when solving optimization problems.

Assume as an example a repetitive analog computer with $T_1 = 2\mu$S, $T_2 = 4\mu$S and $G = 1{,}000$. It is required that $\delta = 0.5$. The values $f_0 = 25$ cps, $t_1 = 0.2$ second, RC = 0.02 second are then obtained.

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Scientific Dept.
Hakirya, Tel Aviv, Israel

[1] I. A. Greenwood, I. V. Holdam, and D. Macrae, "Electronic Instruments," Rad. Lab. Ser. No. 21, McGraw-Hill Book Co., Inc., New York, N. Y. Sec. 4.7 p. 80; 1948.

[2] A. B. MacNee, "Some limitations on the accuracy of differential analyzers," Proc. IRE, vol. 40, pp. 303–308; March, 1952.

Contributors

William J. Bartik (A'48–M'55) was born December 13, 1923, in Philadelphia, Pa. He graduated in 1943 from the University of Pennsylvania with the B.S. degree in electrical engineering. From 1943 to 1948, Mr. Bartik was employed on the research staff of the University of Pennsylvania specializing in the field of electrical noise reduction and measurement. From 1948 to 1950 he was on the staff of Electro-Search specializing in consulting on shielding problems. In 1951 he was employed by Melpar, Inc. and was concerned with communications theory problems. He joined what is now the Remington Rand Univac, Division of Sperry Rand Corp. in 1951, and since that time has been concerned with the development of memory devices. Mr. Bartik is now a project engineer concerned with the development of magnetic core memories.

He is a member of Eta Kappa Nu, Sigma Tau, and Pi Mu Epsilon.

Theodore H. Bonn (S'43–A'45–SM'54) was born May 27, 1923 in Philadelphia, Pa. In 1943 he received the B.S. degree in electrical engineering from the University of Pennsylvania. He was a research assistant at the University until 1946, and from 1946 to 1948 was a development engineer with the Eckert-Mauchly Computer Corp. In 1947 he received the M.S. degree in electrical engineering from the University of Pennsylvania. From 1948 to 1950, Mr. Bonn was chief of the Sonar Components Group at the U. S. Naval Air Development Center in Johnsville, Pa. In 1950 he returned to Eckert-Mauchly as project engineer. He is now head of the Component Research and Development Department of the Remington Rand Univac Division of Sperry Rand Corp. in Philadelphia.

Mr. Bonn was responsible for the development of Unitape, the metallic magnetic tape used with the Univac system. He holds jointly several patents on this development. Mr. Bonn has also been responsible for development of the Ferractor and has a large number of patent applications pending on this development.

He is member of the AIEE, Research Society of America, Tau Beta Pi, Sigma Tau, and Pi Mu Epsilon.

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Ivan Flores (A'51–M'54) was born in New York City in 1923. He received the B.A. degree in mathematics from Brooklyn College in 1948 and the M.A. degree from Columbia University in the same field in 1949. In 1955, he received the Ph.D. degree in the field of supervision in industry from New York University.

Dr. Flores has been working in the field of special purpose computers since 1950. For two years with Mergenthaler Linotype-

Co., Brooklyn, N.Y., he developed circuits for the automatic, electronic justification of typographical materials. Another two years was spent at Balco Laboratories of Newark, N. J. Here he supervised research and development in telemetry and automatic control by digital and analog methods. He also conducted investigations in antenna design and physical chemistry which were his concurrent responsibility. At Nuclear Development Corp. of America he is at present engaged in supervising the design and construction of a computer for complete inventory control of the production and stock of the Otis Elevator Corp.

In the course of his thesis work, Dr. Flores contributed to the application of automatic control in the field of psychological research. The results of the experiments thus conducted will soon appear in the *Journal of Psychology* and the description of the equipment will appear in *Automatic Control.*

❖

Branch P. Kerfoot (S'44–A'49–SM'55) was born in New York, N. Y., on May 9, 1925. In 1945 he received the B.E. degree in electrical engineering from Yale University, and the M.S.E. and Ph.D. degrees from the University of Michigan in 1947 and 1955, respectively.

In 1946 he was on duty in the Navy as an ensign in the engineering division aboard a cruiser. The summer of 1948 was spent as student engineer at the Westinghouse Research Labs., East Pittsburgh, in an airborne radar group. From 1949 to the present he has been with the Missile and Radar Engineering section of the Radio Corporation of America in Camden and Moorestown, N. J. His work has involved design and development of analog and digital data-handling equipments, and he is associated with a computer design group.

He is a member of Sigma Xi and a licensed professional engineer in the state of New Jersey.

❖

Thomas R. O'Meara was born in Kansas City, Mo. in 1924. He obtained the B.S. degree in 1948, and the M.S. degree in 1949, both in electrical engineering, from the University of Illinois. From 1948 to 1955, he was employed at the Radio Direction Finding Research Group at the University of Illinois. He is now employed by the Ramo-Wooldridge Corp. at Los Angeles, Calif.

He is a member of Eta Kappa Nu and Sigma Xi.

❖

John L. Smith was born in Floyds Knobs, Ind., on October 2, 1921. He received the A.B. degree in astronomy from Indiana University in 1942 and the M.A. degree in Astronomy from Indiana University in 1948.

Mr. Smith was a member of the U. S. Naval Observatory from 1942 through 1944. Between 1948 and 1951 Mr. Smith worked in photo-electric photometry at the Lick Observatory of the University of California. In 1951 he joined the Electronic Computers Laboratory of the National Bureau of Standards where he worked on the logical design of several classified computers. As a member of the Digital Systems Section of the Data Processing Systems Division, he participated in developing the logical plans of several large-scale general purpose digital computing systems.

Mr. Smith is a member of Phi Beta Kappa, the Association for Computing Machinery, and the American Astronomical Society.

John Strathman was born in Peoria, Ill. in 1933. He obtained the B.S. degree from the University of Illinois in electrical engineering in 1955. From 1952 until 1955 he was employed at the Radio Direction Finding Research Group at the University of Illinois. He is now serving as an ensign in the United States Navy.

He is a member of Eta Kappa Nu.

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Richard L. Sydnor was born in Milan, Ill. in 1928. He obtained the B.S. degree in 1952 and the M.S. degree in 1953, both in electrical engineering from the University of Illinois. He has been employed at the Radio Direction Finding Research Group at the University of Illinois since 1952.

Mr. Sydnor is a member of Eta Kappa Nu and Sigma Xi.

❖

Arnold Weinberger (S'49–A'50) was born on October 23, 1924. He received the B.E.E. degree from City College of New York in 1950 after serving in the Armed Forces and is currently pursuing graduate studies at the University of Maryland.

In 1950 he joined the National Bureau of Standards Electronic Computers Laboratory where he participated in the SEAC and DYSEAC programs and other logical and systems designs involving digital techniques. On the SEAC, he carried out engineering work concerned with the expansion and operation of the machine. On the DYSEAC, he participated in the development of the logical design of the system, particularly the arithmetic circuitry and the detailed wiring plans from which the machine was constructed.

More recently, he was concerned with increasing computer speed through logical organization of existing circuitry.

Mr. Weinberger is a member of the Association for Computing Machinery.

PGEC News

Elections and Appointments

Results of the election of the new national officers for the 1956–1957 term, and five new members of the Administrative Committee for the 1956–1959 term were announced as follows:

Chairman, J. D. Noe, Stanford Research Institute.

Vice-Chairman, Werner Buchholz, International Business Machines Corporation.

Administrative Committee

J. C. LaPointe,
National Security Agency.

Willis Ware,
Rand Corporation.

Norman Scott,
University of Michigan.

D. C. Bomberger,
Bell Telephone Laboratories.

H. P. Meissinger,
Chicago Museum of Science and Industry.

J. D. Noe announced the appointment of R. Y. Wing, Stanford Research Institute, as Secretary-Treasurer of the PGEC for 1956–1957.

The appointment of Howard Tompkins, Burroughs Corporation, as national chairman of the Meetings Committee was also announced.

New Chapters

The formation of the Montreal, Canada, chapter of the PGEC was announced. Chairman is Harry Schwartz, Electrodesign Corporation, and Secretary is S. Chapin, Sun Life Assurance Company of Canada. An Akron chapter is also in the process of formation. These two chapters will bring the total number of chapters to 16, of which 15 are active. The membership of the PGEC as of April 1, 1956, was approximately 4,000.

Chapter Meetings

San Francisco—Floyd Steel, Litton Enterprises, discussed the Litton Digital Differential Analyzer in March.

Los Angeles—G. B. Greene spoke on the State of the Art of Machine Tool Automation in April.

National Simulation Conference

Climaxing months of preparation, the 1956 National Simulation Conference was held in Dallas on January 19, 20, and 21. The three-day meeting was so well attended that "standing room only" conditions prevailed at some sessions; over 400 persons gathered to hear the 35 technical papers pre-

sented at the Texas Room of the Baker Hotel and the auditorium of the Republic National Bank. Representing universities, government agencies, and industrial concerns of all descriptions, the registrants converged from all parts of the United States; men from Canada and England contributed an international flavor to the highly successful meetings.

The Conference was sponsored by the Dallas-Fort Worth Chapter of the IRE Professional Group on Electronic Computers and the Dallas and Fort Worth Sections of the IRE, together with the North Texas Section of the AIEE and the Dallas-Fort Worth Chapter of the Association for Computing Machinery. A follow-up of the "Cyclone" and "Typhoon" symposia sponsored by the U. S. Navy in New York and Philadelphia in 1951, 1952, and 1953, the 1956 National Simulation Conference was the first public meeting of national scope specifically devoted to simulation and related computing techniques. It is expected that the Conference will now become an annual affair, in Dallas or elsewhere.

Simulation embraces the use of computers to simulate a system, device, or process (be it electrical, mechanical, chemical, economic, or whatever) by establishing an electronic circuit (for example) which has the same mathematical equations of behavior as the system, device, or process under study. Measurements made on the simulated system are then related to the actual system. *Mathematical* simulation is the use of the computer purely as an equation solver; the problem may be handled on a slowed or speeded time scale if more convenient than real time. *Physical* simulation is the use of the computer to take the place of a component or subsystem, not yet fully designed or not yet available, in a test of an over-all system; in this case the computer must operate on real time and its inputs and outputs must be compatible with other elements of the over-all dynamic system.

The technical papers presented at the Conference dealt with equipment, techniques, and computer applications in both the mathematical and physical simulation fields; both analog and digital aspects were included. The range of applications included army tanks, gas turbines, guided missiles, radar, torpedoes, and medicine. Computation equipment emphasis was placed upon the design of function generators, operational amplifiers, and servomechanisms. The complete technical program was outlined in the January, 1956 issue of PROCEEDINGS OF THE IRE. All of the papers presented will be published collectively in a PROCEEDINGS volume; the PROCEEDINGS can now be ordered from the Conference Treasurer, Professor F. W. Tatum, Electrical Engineering Department, Southern Methodist University, Dallas, Texas.

On Friday evening, January 20, 1956, almost 200 of the Conference visitors toured the electronic computer facilities, both analog and digital, of Chance Vought Aircraft Inc., Dallas, and Convair, Fort Worth. Constituting two of the larger electronic computer facilities of the United States, these installation tours afforded the visitors an opportunity to become acquainted firsthand with equipment and techniques in current use.

Nor was the social side neglected at the Conference. On Thursday evening, January 19, 1956, a Reception was held for Conference registrants, their wives, and guests, at the Baker Hotel. At the Reception, sponsored by the Western, Eastern, Midwestern, and Southeastern Simulation Councils, informal individual get-togethers were the rule. However, a representative of each Council presented a brief description of the activities and plans of his Council.

WESTERN JOINT COMPUTER CONFERENCE

The Western Joint Computer Conference and Exhibit was held in San Francisco, February 7–9, 1956. The three-day session was managed by Chairman Oliver Whitby of Stanford Research Institute and keynoted by N. H. Taylor, Computer Systems Engineer with the Lincoln Laboratory, Massachusetts Institute of Technology. Mr. Taylor reviewed the development of the automatic computer industry from infancy to its present early adolescence and then gave some predictions of things to come. Among these was the prediction that within the next ten years computers will automatically control all transport aircraft with the pilot acting as moderator.

A number of sessions on programming and coding of large scale scientific and business computers included a number of papers on automatic programming and supervising systems, emphasizing those techniques which will be helpful in applying computers to business problems. A team of RCA engineers described the new BIZMAC computer system which has recently been installed for military inventory control.

Novel uses of digital computers as simulators for studying traffic control systems, planning new roadways, and baseball forecasting were described.

Papers on analog computing techniques included several on combined analog and digital systems.

Among papers describing new advances in hardware were descriptions of auxiliary equipment such as magnetic recording heads, the relatively new Charactron display tube, new magnetic tape handles, and a system for data transmission over telephone circuits. Among new circuit components described is a device known as the *transfluxor*. This can best be described as a variable setting magnetic gate in contrast to the customary bistable devices used in computer design.

Copies of the proceedings will be available through the three sponsoring organizations: The American Institute of Electrical Engineers, The Institute of Radio Engineers, and The Association for Computing Machinery.

MEETINGS

International Congress on Automation

The International Congress on Automation, organized by the Department of Mechanics of the Conservatoire National des Arts et Métiers, Ministry of Public Education, with the assistance of several scientific and engineering associations and with the help of the Association Française pour l'Accroissement de la Productivité, will be held June 18–24, 1956, at the Conservatoire National des Arts et Métiers, 292, rue Saint-Martin, Paris.

Automation will be studied under its theoretical and practical aspects. The aims of the Congress are to show the various aspects of "General Automation" and its conditions of applications (scientific, technical, economical, and psychological). The Congress will not consider all the aspects of automation, especially all the specific technological aspects.

In addition to the Congress an exhibition organized with the help of UNESCO and the assistance of Association pour l'Accroissement de la Productivité (AFAP) will be held permanently at the Conservatoire National des Arts et Métiers. Motion pictures on automation will be shown continuously.

Ladies are cordially invited to attend the Congress. Special programs and visits of Paris and suburbs will be organized for their entertainment.

WESCON

The 1956 Western Electronic Show and Convention will be held at the Biltmore Hotel, Los Angeles, August 21–24, 1956.

ACM ANNUAL MEETING

The Association for Computing Machinery will hold its Eleventh Annual Meeting on the Westwood campus of the University of California at Los Angeles, August 27–29, 1956. Local arrangements will be under the direction of Dr. Gilbert King, International Telemeter Corporation. Correspondence concerning arrangements should be addressed to the Association for Computing Machinery, Box 3251 Olympic Station, Beverly Hills, California.

STANLEY B. DISSON
News Editor
Burroughs Research Center
Paoli, Pa.

Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.—*H. D. Huskey*

GENERAL

681.142:621.3.078/.079 56-53

Industrial Uses of Special-Purpose Computers—A. H. Kuhnel. (*Instruments and Automation*, vol. 28, pp. 1108–1113; July, 1955.) An account is presented of the analysis of a simple machine-control problem and the design of a suitable special-purpose computer to perform the task. Economic factors are also briefly considered.

Courtesy of PROC. IRE and *Wireless Engineer*

56-54

Computers Challenge Engineering Education—F. C. Lindvall. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 41–43; 1955.) The author is preoccupied with the question of having superficial trends invade the field of engineering education. He correctly emphasizes the importance of fundamentals in scientific and engineering training, even in view of the glamorous inducements offered by the automatic computer. The fact remains, however, that the computing machines have radically altered the role of such basic subjects as mathematics, which the writer does not point out with sufficient clarity. Nor does he indicate that these basic changes will necessitate substantial curriculum revisions. To the reviewer's mind the author could have emphasized the effect of automatic computers on the engineering profession itself. The direct application of basic sciences to the solution of problems can now be carried out. In other words, the days of the handbook engineer are rapidly coming to an end. The wider use of basic sciences in all areas of industrial and business activity requires that a larger number of our people be trained in the basic sciences. The author would have done well to point out the great need for improved mathematics education in our schools and colleges in order to supply this rapidly mounting need. The reviewer believes that the discussion of what should be taught in schools and what should be left for the engineer to learn in industry will be properly resolved only when more intimate and continuing relations are established between industry and colleges. This can be achieved through closer cooperation between industrial and educational institutions.

Arvid W. Jacobson

621.37:621.318.57 56-55

The Folded Tree—A. W. Burks, R. McNaughton, C. H. Pollmar, D. W. Warren, and J. B. Wright. (*J. Franklin Inst.*, vol. 260, pp. 9–24, 115–126; July, August, 1955.) The problem of constructing circuits to perform certain functions, such as switching functions, is treated by representing the circuits by "vertex diagrams," of which the "folded tree" is a particular form.

Courtesy of PROC. IRE and *Wireless Engineer*

56-56

Coding a General-Purpose Digital Computer to Operate as a Differential Analyzer—R. G. Selfridge. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 66–72; 1955.) A system is described in which the various functions of an analog differential analyzer become elements of a pseudocode which may, with an appropriate interpreter routine, be processed by a general purpose digital computer. The analog coding for a differential equation may thus be directly transformed into a digital code. The computers actually employed are an IBM 701 and a REAC. The functions included are integration (employing Simpson's Rule), addition, variable and constant multiplication, division, and certain relay operations such as the generation of discontinuities. The author states that longer running times are required for digital solutions; however, for all but the simplest problems, digital methods require less over-all time in addition to being more accurate and applicable to a wider range of problems. No attempt is made in the article at a comparison between this type of interpreter and more conventional coding schemes for the digital solution of differential equations.

Max Palevsky

56-57

The Integrated Use of Analog and Digital Computing Machines for Aircraft Dynamic Load Problems—B. Mazelsky and R. F. O'Connell. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 66–72; 1955.) This article does an excellent job of depicting the complexity of the type of problems faced by aircraft designers. It points out that, during the preliminary design stage, an analysis must be made with rather sketchy data. At this stage the investigation requires the determination of those parameters of the system that are most critical. Such a method requires the very rapid exploration of a large number of parameters. This investigation is best accomplished by the use of computers, both analog and digital, exploiting the virtues of each. This article emphasizes that the solution of engineering problems on computers is more than that of effecting certain calculations, but involves the choice of the best method feasible, taking delivery schedules into account. The authors describe several methods used in solving such problems, indicating the virtues and faults of each method, especially in terms of the characteristics of the machine used to solve them. Finally there is a description of the use of an analog and a digital machine, each solving the same problem; that is, a tail symmetric flutter analysis of a transport type aircraft. The results show remarkable agreement between solutions obtained on the two machines, demonstrating great skill in the integrated use of analog and digital computers.

William J. Schart

56-58

A High-Speed Multichannel Analog-Digital Converter—James M. Mitchell. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1945, Los Angeles, Calif.*, pp. 118–127; April, 1954.) The system described in this paper takes the dc output (in the low millivolt range) of 400 strain gages for each of twenty structural loads. A commutator samples and programs the recording. One hundred channels are recorded on nine tracks during each twenty-five revolutions of the converter's magnetic drum (3,500 rpm). Total time required for one conversion, with two-decimal-digit output, is 132 microseconds. The elements of the system are a pulse source, a modulator, an amplifier and filter, a phase discriminator, summing networks, and logical circuits. All are described in considerable detail. The conversion is accomplished in sixteen time intervals defined by a four-stage binary counter. The binary code used for decimal digital output is 5-2-1-1. The statement is made that any computer code may be used by changing the value of the summing resistors. The number of significant digits can be increased by utilizing the time intervals not in use. The author states that preliminary experiments indicate that a clock frequency of 0.5 megacycle may be practicable. Since the appearance of this paper the converter has been improved. The successor to it is reported on in the ONR "Digital Computer Newsletter," reprinted in the *J. Assoc. Comp. Mach.*, vol. 3, pp. 55–56; January, 1956. The new model performs up to 100,000 conversions per second with thirty-millivolt resolutions and 0.1 per cent guaranteed accuracy. It is available with a high-speed input commutation switch, digital output magnetic recorders, and programming circuits.

A. Dowling

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—The Editor

56-59

A New Approach to Grounding in DC Analog Computers—C. M. Edwards. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 23–26; 1955.) Conventional grounding methods require a considerable amount of copper in the ground bus in order to keep bus voltages within acceptable limits. The author proposes a grounding system in which three ground buses are used: *i.e.*, 1) a chopper ground, 2) a cathode return bus, and 3) a potentiometer ground bus. Since relatively small currents are flowing in buses 1) and 3) and these grounds are of most importance to computational accuracy, a marked reduction can be made in the amount of copper required in the grounding system. Throughout the paper the author is concerned with low-frequency phenomena and pays particular attention to the elimination of offset voltages due to poor grounding techniques. This new approach to the grounding problem has been used in a computer installation and appears to be practical and effective.

D. T. Greenwood

ANALOG EQUIPMENT

56-60

Simplified Analog Computer—V. B. Corey. (*Electronics*, vol. 29, pp. 128–131; January, 1956.) The Donner (Donner Scientific Company) analog computer is described. The computer is an electronic differential analyzer having ten identical operational amplifiers and a detachable board for problem set-up. The author claims that although the computer sacrifices extreme accuracy and elaborate design, it is sufficiently versatile to handle the most complex problems. He also states that investment and operating economy are comparable to those of a desk calculator. The characteristics and theory of operation of the unit are given including a schematic and description of the dc operational amplifier. The computer finds application in industry and the laboratory, and with accessory equipment can be adapted for the solution of general nonlinear problems.

Norman F. Loretz

681.142:621.383.2 56-61

Photoelectric Transformation of Mathematical Functions. Solution of Equations—G. Blet. (*Bull. Soc. Franç. Élect.*, vol. 5, pp. 341–344; June. 1955.) An arrangement comprising a mirror galvanometer in combination with an appropriately shaped diaphragm and a photocell is used to generate a current $f(x)$ when the current x flows through the galvanometer. Elaboration of the arrangement to generate complex functions is discussed.

Courtesy of Proc. IRE
and *Wireless Engineer*

681.142:621.383 56-62

A Photoelectric Analog Computer for Investigating the Dynamic Behaviour of Linear Systems—S. Kitsopoulos. (*Bull. Schweiz. Elektrotech. Ver.*, vol. 46, pp. 690–693; July 23, 1955.) Apparatus is described for determining the output function of a linear system such as an amplifier or servomechanism when the input and transfer functions are known. The two known functions are represented by appropriately shaped apertures in diaphragms interposed between light source and photocell; the mechanical system used to produce the required continuous variation of the input function is described in detail.

Courtesy of Proc. IRE
and *Wireless Engineer*

56-63

A High-Speed Correlator—H. Bell Jr. and V. C. Rideout. (Trans. IRE, vol. EC-3, pp. 30–36; June, 1954.) The article describes a high speed analog type correlator for use in obtaining auto and cross-correlation functions of electrical signals. The device is capable of handling signals having frequency components up to approximately 15 kc. It can obtain 41 discrete points on a correlation curve in five seconds. The delays are introduced by means of a tapped artificial delay line using M derived sections having a maximum delay of 2080 microseconds. Multiplication is accomplished by means of a commercial analog multiplier unit.

Jerome B. Wiesner

UTILIZATION OF ANALOG EQUIPMENT

681.142 56-64

High-Speed Electronic-Analog Computing Techniques— D. M. MacKay. (*Proc. IEE*, Part B, vol. 102, pp. 609–620; September, 1955. Discussion, pp. 620–623.) An investigation has been made of the upper limits of speed conveniently attainable in various basic operations performed with a particular differential analyzer. With multidimensional displays and electronic programming a very large increase in information capacity is attainable in problems requiring systematic search processes for their solution.

Courtesy Proc. IRE
and *Wireless Engineer*

56-65

Polynomial Root Solving on the Electronic Differential Analyser—Cyril Atkinson. (*MTAC*, vol. 9, pp. 139–143; October, 1955.) This paper presents a technique for finding real or complex zeros of polynomials having real coefficients. The (constant) value of the nth derivative is fed into an integrator. The ouput, coupled with the initial value of the $(n-1)$st derivative, is fed into another integrator and this process is continued until the polynomial is obtained and plotted to show the real zeros. Complex zeros can be obtained by setting $f(x+iy)=U(x, y)+iV(x, y)$. A guess is made for y, and U and V are generated by summing powers of y multiplied by the corresponding derivatives of $f(x)$. If $U=V=0$ for some x, then $x\pm iy$ are a pair of conjugate complex zeros. Examples are given for real zeros of a quintic, and complex zeros of a quartic and a sextic polynomial. It is not clear in these examples just how the correct value for y was chosen.

John Selfridge

DIGITAL COMPONENT RESEARCH

621.373.43:621.385.15 56-66

Secondary-Emission-Valve Pulse Generator with Cathode Output—R. Favre. (*Helv. Phys. Acta*, vol. 28, pp. 167–171; May 31, 1955. In French.) A positive-feedback circuit giving a very low output impedance is used, capable of producing pulses of amplitude 50–60 v with rise time about 20 mμs. By suing a pentode as cathode load it is possible to obtain a wide variety of pulse waveforms. The arrangement gives a better performance than the ordinary blocking oscillator.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.374.32 56-67

High-Frequency Pulse Counter—R. Favre. (*Helv. Phys. Acta*, vol. 28, pp. 179–184; May 31, 1955. In French.) A circuit based on the secondary-emission-tube pulse generator described in 56-66 above.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.373.431.1:621.373.44 56-68

Investigation of the Time Delay in the Triggering of a Pulse in a Monostable Multivibrator—G. Haas. (*Arch. Elekt. Übertragung*, vol. 9, pp. 272–276; June, 1955.) Results of experiments indicate that a monostable multivibrator may be used as a pulse amplifier in applications where waveform distortion is unimportant. With pulse voltages above 100 mv the multivibrator used showed time delays of less than 10^{-8} seconds and these were independent of pulse width over a wide range. The gain obtainable is about 500. Time delays in a free-running multivibrator are of the order of 10^{-8} to 10^{-6} seconds; this is shown theoretically to be due to the stray capacitances present.

Courtesy of Proc. IRE
and *Wireless Engineer*

621.373.431.2:621.373.52:621.314.7 56-69

Junction-Transistor Blocking Oscillators—J. G. Linvill and R. H. Mattson. (Proc. IRE, vol. 43, pp. 1632–1639; November, 1955.) Circuits have been designed producing pulses with rise times <0.1 μs, using transistors with α-cut-off frequencies of a few mc. Details of the regenerative transformer coupling are discussed. Triggering requirements and the effects of loading are evaluated. Experimental results support the theory.

Courtesy of Proc. IRE
and *Wireless Engineer*

56-70

A Set of Transistor Circuits for Asynchronous, Direct-Coupled Computers—R. A. Kudlich. (*Proc. Western Joint Computer Conf., Los Angeles, Calif.*, pp. 124–129; 1955.) In the design of circuits for asynchronous machines, considerable variation in the rise time of the individual circuits can be tolerated. As a result, a wide variation in circuit parameters is allowable provided this variation can be taken into account in the design of the circuit. Although the circuits described in this report may be of little

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—*The Editor*

value at this later date, the design method is of considerable interest. It differs from more usual designs in that the results are presented as a function of the limiting values of the transistor parameters rather than of typical values. The graphical representation of the two extreme characteristics are superposed on the same plot. From this, inequalities are written which express the range of values of the circuit elements as a function of the maximum and minimum values of the transistor parameters. The example given is that of the design of a two transitor flip-flop using point contact transistors. Unfortunately, the graphical representation used was the conventional "*n*-characteristic" which, as the author indicates, is not a sufficiently good approximation for a majority of the available transistors. As a result, the resulting circuit is not necessarily a good design for all values of parameters within the expected range. It is worth noting that, since there are better graphical representations available for junction transistors, this method should produce good results when used with them.

Gordon Morrison

56-71

A "One Turn" Magnetic Reading and Recording Head for Computer Use—D. F. Brower. (1955 IRE Convention Record, Part 4, pp. 95–100; 1955.) An interesting evolution of magnetic read-and-write heads for digital use is described, using ferrite as magnetic path, and initially using a one-turn ribbon of silver foil as winding. An "early" version has an external transformer with totally enclosing ferrite "cup" cores to get a suitable impedance ratio between signal source and head; connection between head and transformer being via bifilar conductor straps. Excellent shielding contra cross-talk with close head spacing is claimed. A "later" version employs a high-impedance winding directly upon the ferrite core of the head, and the one-turn winding is degenerated into an eddy-current shield wrapped about one leg of the core; for this some obscure hybrid merits are implied due to its vestigial properties as a "winding." With equal writing current, about twice this readout voltage is indicated in comparison to a "conventional" head. The design of magnetic heads involves many interdependent and inconstant parameters, and in the particular direction of attack described this seems to have been done with considerable ingenuity. The result may well represent an improvement for many applications, but the qualitative arguments and data presented are so unconvincing and incomplete as to leave this reader in considerable doubt as to what has been gained. For example, the new heads are compared to an unspecified "conventional" head apparently without shielding or eddy current gap-spacer, so that "at best 50 per cent of the flux is wasted" whereas "all of the flux produced in the single-turn head is forced to pass outside this head," presumably by the ribbon "winding" playing the same role. To insist upon calling the "later" version of head an "integral-transformer" and "single turn" device seems rather a tour-de-force as it is simply a neat, compact (and probably quite efficient) wound-leg *U* of fermite provided with good eddy-current shielding. No reference is made to any of the extensive prior literature on heads and magnetic recording.

J. H. Bigelow

538.221:681.142 56-72

Ferromagnetic Computer Cores—C. F. Devenny, Jr., and L. G. Thompson. (*Tele-Tech & Electronic Ind.*, vol. 14, pp. 58–59, 94; September, 1955.) Recent improvements in the properties of rectangular-hysteresis-loop cores are illustrated by characteristic curves relating to 4–79 permalloy and 48 per cent Ni-Fe alloy tape cores.

Courtesy of Proc. IRE and *Wireless Engineer*

681.142:621.3.042 56-73

Logical and Control Functions Performed with Magnetic Cores—S. Guterman, R. D. Kodis, and S. Ruhman. (Proc. IRE, vol. 43, pp. 291–298; March, 1955.) This article describes briefly the basic principles involved in using magnetic cores in shift registers and for logical and control functions, but is principally devoted to description of a specific method for developing certain logical functions using the primitive terms, "AND, OR, and INHIBIT," with the latter further defined as "AND NOT." The authors describe these terms as "the three elementary logical operations," which is an arbitrary statement. For one input there are four possible elementary logical operations, and for two inputs there are sixteen possible elementary logical operations. In theoretical propositional calculus all possible operators may be synthesized from either of two primitive terms, the matrices of which are as follows:

S	0	1
0	1	0
1	0	0

D	0	1
0	1	1
1	1	0

This was first demonstrated by Sheffer (*Trans. Amer. Math. Soc.*, vol. 14, pp. 481–488; 1913). It has also been shown that, in logical structures composed of magnetic elements of the type described, it is necessary to have only some element (there are several) that contains negative coincidence (responds with a 1 output to the coincidence of 0's on each of its two inputs) and some other appropriate element to provide for the time delay problems, such as a magnetic core mixer which in this article is described simply as OR, with the "inclusive" character of the element (as opposed to "exclusive-OR") assumed. In the "Conclusions," the authors carefully, and properly, state, "The circuits presented in this paper are by no means the best, the most economical, or the only possible ones for solving these particular problems." Reference is made in the article to work done at 300 kilocycles with the comment that the maximum frequency of reliable core circuitry is below one megacycle. It is quite possible that ultimately magnetic core operation at one megacycle or higher will be practical, but most workers in this field have found that many not-obvious problems plague them at the higher frequencies and there are so many useful applications at 100 kc or so, that it may be desirable to concentrate on solving basic problems to the point of full-scale utilization of the principles at moderate frequencies. Again, in the conclusions, the authors indicate that the reliability of such systems is high because of the stability of the magnetic cores and the relatively few electron tubes required. This comment passes over the question of diodes so lightly that they are not even mentioned. The reviewer knows of no techniques that do not require the use of diodes, and none are shown in this article. The reliability of the diodes in complex matrices seems to the reviewer more significant than the cores or the few electron tubes, and in practice has appeared to be the principal limiting factor with regard to long-term stability. It may be that the diode question can be eliminated by special circuit designs, or that diodes exist with greater reliability than the reviewer realizes; but unless such circuitry is shown or such diodes are described, the problem deserves mention. Several interesting arrangements of elements are shown for counters, adders, multipliers, and the like. Under "limitations," the second note states that the technique "being sequential in nature, is not very well suited for parallel operation." Either the reviewer does not understand this or does not agree with it, or both. Undoubtedly, these authors have done considerable work in this field since the date of this article and their future activities should result in publications of interest.

John D. Goodell

538.221:539.234 56-74

Preparation of Thin Magnetic Films and Their Properties—M. S. Blois, Jr. (*J. Appl. Phys.*, vol. 26, pp. 975–980; August, 1955.) Evaporation technique is described for producing films of ferromagnetic material, particularly Ni-Fe alloys, with thicknesses from 1,000 Å to 100,000 Å and coercivities of 0.1-40 oersted. Magnetic orientation is used to produce a rectangular hysteresis loop. Questions of suitable substrate materials, evaporable dielectrics for use in insulating multilayer films, and control of alloy composition are discussed.

Courtesy of Proc. IRE and *Wireless Engineer*

56-75

A New Nondescriptive Read for Magnetic Cores—R. Thorensen and W. R. Arsenault. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 111–116; 1955.) A method for nondestructive readout of coincident current magnetic storage cores is described. Each ferrite memory core is to have a radial hole through which an interrogation current pulse can pass. This current disturbs the residual flux in the core and consequently will induce a signal in an output winding. This output signal is only dependent upon the direction of residual flux. Laboratory tests are reported which indicate the feasibility of this mode of operation; and interrogation cycles of 0.5 micro-

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second are mentioned. The residual flux under the tests described is reduced by approximately two-thirds due to the interrogation pulses, although the peak readout signal amplitude decreases only slightly. The experiments were carried out on General Ceramics size F-262 toroidal cores in which the aperture is made by drilling.

A. S. Hoagland

56-76

Experiments on a Three-Core Cell for High-Speed Memories—J. Raffel and S. Bradspies. (1955 IRE CONVENTION RECORD, Part 4, pp. 64–69; 1955.) This paper describes a type of magnetic-core memory which uses three ferrite cores per bit of storage rather than one as in the conventional coincident-current memory. This permits the separation of the selection function from the storage function and removes the limitation normally imposed by the knee of the hysteresis loop on the maximum value of half-current excitation. Thus, larger currents may be applied to the memory core and the switching time thereby reduced. Another advantage is a reduction of noise output from the unselected cores. The method has the disadvantages of greatly increased wiring and circuit complexity however. It is suggested that this method will find greatest use in small memories where speed is the determining consideration. The authors report that, for a single bit, a voltage ratio of 15 to 1 was obtained between the ONE and ZERO outputs and that the cycle time was 0.4 microsecond. Plans have been made to construct a 256 bit memory of this type.

Charles E. Pallas

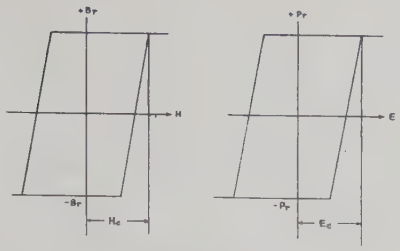
537.227:546.431.824-31 56-77

Electrical Behaviour of Barium Titanate Single Crystals at Low Temperatures—H. H. Wieder. (*Phys. Rev.*, vol. 99, pp. 1161–1165; August 15, 1955.) Measurements were made over a temperature range including the phase transitions from tetragonal to orthorhombic at −5°C and from orthorhombic to rhombohedral at −92°C. As the temperature decreases through a transition, the coercivity, polarization-reversal time, and spontaneous polarization decrease discontinuously. Dielectric constant varies linearly with switching time; this supports the theory of a relaxation mechanism for polarization reversal.

Courtesy of PROC. IRE and *Wireless Engineer*

56-78

Memory Matrix Using Ferroelectric Condensers as Bistable Elements—Charles F. Pulvari. (*J. Assoc. Comp. Mach.*, vol. 2, pp. 169–185; July, 1955.) To a great extent the ferroelectric material is the electrical analog of the ferromagnetic material. The following *B-H* and *P-E* hysteresis loop (Fig. 1) illustrate their similarity. In order to use ferroelectric material as a memory element, it should have properties comparable to those required for magnetic storage namely: a) high retentivity of polarization, b) high nonlinearity of the dielectric hysteresis loop, c) switch speed in the mega-



Br = Remanent magnetization
Pr = Remanent polarization
H = Magnetic field intensity
E = Electrical field intensity
H_c = Magnetic coercive force
E_c = Electric coercive force

Fig. 1.

cycle range. While the hysteresis loop of perfect single crystal plates of $BaTiO_3$ is practically a rectangle, and most desirable for memory application, the material used by the author consisted of thin sheets of recrystallized $BaTiO_3$ which are much easier to obtain than single crystal plates of $BaTiO_3$. Because the essential parameters of this material were not uniform, the author successfully built 10×10 memory matrix using individually and properly selected condensers each of which has an area of 1 square mm with 3 ml thick recrystallized $BaTiO_3$ as the dielectric material. The matrix was tested successfully with pulse durations between 2.0 and 0.5 microseconds. Signal to noise ratios of 2 or better were obtained. Because of the selection index available (degree of nonlinearity) the author showed that for this material a 10×10 matrix is about the largest practical size for satisfactory operation.

J. C. Chu

DIGITAL SYSTEM RESEARCH

681.142:621.318.5 56-79

A Method for Synthesizing Sequential Circuits—G. H. Mealy. (*Bell Syst. Tech. J.*, vol. 34, pp. 1045–1079; September, 1955.) A theory is developed from design procedures suggested by Huffman (*Jour. Franklin Inst.*, vol. 257, pp. 161–190, 275–303; March/April, 1954) and Moore (to be published in *Automata Studies*, Princeton Univ. Press) enabling intricate relay systems to be built up from an initial diagrammatic statement of the essential requirements. By successive application of simplifying reductions a unique circuit is finally obtained.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142 56-80

Improvement of an Iteration Process Suitable for Automatic Division—C. Böhm. (*Ricerca Sci.*, vol. 25, pp. 2077–2080; July, 1955.) Electronic computers having no organ of division are provided with a subroutine for the computation of reciprocals. An improvement of this subroutine is proposed which permits a reduction of about thirty per cent in the number of operations without affecting the accuracy.

Courtesy of PROC. IRE and *Wireless Engineer*

DIGITAL EQUIPMENT

56-81

An Electronic Digital Polynomial Root Extractor—R. R. Johnson. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 119–123; 1955.) A special purpose digital computer capable of extracting the complex roots of polynomials up to the 16th degree is described. The mathematical method used is a repeated evaluation of the polynomial in the direction of a reduction in its absolute value. The direction decision is made by the machine. A solution time of approximately 16 seconds per root is achieved. A certain amount of normalization of the coefficients of the polynomial and its derivatives is necessary before the numbers are put into the computer. This work is done by hand, to avoid increasing the complexity of the computer, whose arithmetic operations are limited to add, subtract, shift, and bit sequence inversion. Input is bit by bit, using a pair of manually operated switches, and output is visible on an oscilloscope. A very complete description is given of the mathematical formulation of the problem, and the logic of the computer, which uses 20 flip-flops and approximately 200 germanium diodes in conjunction with a small magnetic drum memory. The published photograph shows a rather neat, compact job of packaging. The author reaches some conclusions about the advantages of a special purpose computer with which the reviewer is forced to disagree. The author claims that "where there is need for its special purpose, the ready availability of the computer and its ease of programming make it a valuable scientific tool." However, had he been willing to construct a medium-speed, general purpose machine he would have merely doubled the amount of equipment with a consequent gain of far more than two in versatility and capability. His problem would then have been one of coding a program for the specific application to his problem. The computations preparatory to input which he is forced to make with the present computer would be avoided. The author weakens his own argument as to the value of a special purpose machine by devoting two paragraphs to suggestions as to other possible applications!

F. H. Hollander

56-82

LGP-30 General Purpose Digital Computer—S. Frankel and J. Cass. (*Instruments and Automation*, vol. 29, pp. 264–270; February, 1956.) After an introduction giving a partial history of universal computers, the article gives some criteria for judging general purpose computers. These include speed of computations, speed of programming, cost, and reliability. A factor influencing the latter is the number of components. The LGP-30 is then described. A serial type, stored program computer, it uses a magnetic drum type memory storing 4096-32 bit words. One of the 32 bits is not used and one is used for sign. A standard Flexowriter, including the punched tape equipment, is used for input and output. Al-

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—*The Editor*

though some of the alphabetical characters are used for programming, the article is not explicit as to whether the computer is alphanumeric. A rather conventional command list of sixteen commands is described. A somewhat unique command which appears quite useful is one for marking the exit point of a routine for later return to that point. Output is controlled by commands which result in one character typeout per command. Justification for this procedure is attempted by an argument concerning lack of format control in other procedures. In conclusion, a sample subroutine is written and described which calculates a sine of an angle in the first quadrant in some 0.13 seconds using twenty commands and ten other memory locations.

L. S. Michels

56-83

A Note on the Electronic Computer at Rothamsted—S. Lipton. (*MTAC*, vol. 9, pp. 69–70; April, 1955.) This note gives a short description of the "401" experimental computer at the Statistical Department at Rothamsted Experimental Station (England) and an indication of the type of work being carried out on the machine. The 401 is a serial computer with a word length of 32 binary digits which adds or subtracts in 100 microseconds. There are 23 tracks of 128 words each on a magnetic disc. Seven of these are always available, and one of the remaining 16 is selected by high-speed relay switching. The arithmetic unit uses a two-address code and has five available registers. Multiplication takes 32 add times; shifting n places takes n add times. There are collation and comparison orders, but no division order. Routines for analyzing randomized blocks and Latin square experiments have been used, and routines for the analysis of factorial experiments are in progress.

John Selfridge

UTILIZATION OF DIGITAL EQUIPMENT

56-84

The Need for Integration of Accounting Systems and the Design of Electronic Data-Processing Systems—P. Kircher. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 26–28; 1955.) Accounting systems and electronic equipment must be integrated *in the design stage* for really effective use. To this end, electronic designers are improving their equipment, and accountants are making a real effort to become acquainted with the abilities of electronic machines, and to make their systems more compatible with the abilities of electronic equipment. Past experience has now shown the folly of using the equipment as a service center for present systems, of doing the toughest problems first, of buying equipment because everybody's doing it, or of confining the equipment to certain limited applications. To make intelligent use of electronic equipment, management must have new insights into their needs for information and communication, obtained through the new interest in management science, operations research, and mathematical programming. Then they must use the new equipment imaginatively to produce the information they need. This can be done through good systems design which integrates not only within a function, but between functions. The whole operation should be guided by top management, and the systems design must meet their requirements.

R. L. Sisson

56-85

Data-Processor Requirements in Production and Inventory Control—H. T. Larson and A. Vazsonyi. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 48–61; 1955.) The authors present the development of a mathematical model for representing the "explosion" of parts lists in production planning operations. They show that the requirements for parts can be represented in matrix form, and that familiar matrix manipulation operations may be used. An advantage of the matrix representation is that the whole operation can be communicated between mathematicians more precisely than by normal quantitative statements. However, it appears that the final result of the operation is the same as that obtained by the more conventional methods now used by production management; no optimization of production planning decisions or reduction in cost of making those decisions is claimed. The paper discusses the magnitude of the computational problem involved when using this method. The authors argue for new logical designs for computers, so as to be able to handle the problem efficiently. For instance, there are numerous searching (table look-up) operations where a table is searched for a desired part number. In one such operation, assuming a 5-ms average access internal memory (drum) a single table look-up may require from 25 minutes to 25 hours for three company sizes presented in the paper. The authors suggest the desirability of a 50 microsecond access time, 60,000 digit storage system for such operations, plus a back-up of 200,000 digits of medium-access storage, to reduce this searching time. The paper is significant in that it examines an old problem in a new light. It is of interest to learn the price that must be paid in computation time when approaching the production planning operation from this point of view. Also, it seems possible that the technique might someday be applied to more aspects of production control and thus obtain more of the potential benefits from the different by-products resulting from this type of formulation.

R. G. Canning

681.142 56-86

An Attempt to Simplify Coding for the Manchester Electronic Computer—R. A. Brooker. (*Brit. J. Appl. Phys.*, vol. 6, pp. 307–311; September, 1955.) Two main simplifications are made, both at the cost of increased machine time. To ensure that all quantities involved in a calculation are represented to the required degree of accuracy, every number occurring is associated with its own scale factor. Again, in using the two levels of storage provided, arrangements are made so that "instructions" are written out as if for a one-level store. A program in the simplified form is described.

Courtesy of PROC. IRE and *Wireless Engineer*

56-87

Analysis of Problem Codes on the MANIAC—E. H. Herbst, N. Metropolis, and M. B. Wells. (*MTAC*, vol. 9, pp. 14–20; January, 1955.) A routine called the "Code Analyzer" has been developed to give a static and a dynamic count of the various orders used in any problem code or subroutine. To make the dynamic count, an interpretive routine is necessary which occupies a section of the electrostatic memory chosen so as not to conflict with the numerical storage of the code being analyzed, the latter having been stored on the drum. Tables are given of analyses of a problem in hydrodynamics, a Monte Carlo problem, a problem in mathematical logics, and a summary of the analyses of 37 subroutines. A brief description is given of the MANIAC vocabulary symbols. The unit of time used is not specified, but presumably it is the millisecond, and the interpretive routine operates approximately 1/200 as fast as the original code.

John Selfridge

56-88

Coupon Collector's Test for Random Digits—Robert E. Greenwood. (*MTAC*, vol. 9, pp. 1–5; January, 1955.) Beginning at a specified position in a series of digits, count the length of a sequence necessary to include all ten distinct digits. The distribution of these lengths for different initial positions give a test for randomness called the coupon collector's test. A table is given of the probabilities associated with sequence lengths 10 to 75. In applying this test to the digits of π and e, it was considered advisable to make the sequences nonoverlapping to avoid dependence among the set of sequence lengths. The results are tabulated for the first 2020 and 2486 digits of π and e, respectively.

John Selfridge

537.533 56-89

Numerical Ray Tracing in Electron Lenses—J. C. E. Jennings and R. G. Pratt. (*Proc. Phys. Soc.*, vol. 68, pp. 526–536; August 1, 1955.) Corrections are suggested to Liebmann's formulas for tracing paraxial rays (*Proc. Phys. Soc.*, vol. 62, pp. 753–772; December 1, 1949); a more accurate method is developed, applicable also to marginal rays, and is compared with methods suggested by other workers. The use of the constancy of the Wronskian determinant as a criterion of accuracy of paraxial ray tracing is discussed.

Courtesy of PROC. IRE and *Wireless Engineer*

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—*The Editor*

56-90

The Laminar Boundary-Layer Equation: A Method of Solution by Means of an Automatic Computer—D. C. F. Leigh. (*Proc. Camb. Phil. Soc.*, vol. 51, pp. 320–332; April, 1955.) The incompressible laminar boundary layer equation was solved on EDSAC by a numerical method, the basic feature of which was the simultaneous adjustment of values along a line in the y-direction (perpendicular to the stream) given values upstream of this line. Successive adjustments were made by a matrix method exhibiting excellent stability properties. A solution to six decimals was obtained in the upstream neighborhood of the separation point, but attempts to integrate through separation confirmed the existence of a singularity there.

Stanley Gill

56-91

Pattern Recognition and Modern Computers—O. G. Selfridge. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 91–93; 1955.) Pattern recognition is defined as extraction of significant features from a background of irrelevant detail. Several examples help stress that "significant" is the critical word. A suggested machine model is capable of performing a number of separate operations; *e.g.*, averaging (emphasizing local homogeneity), or edging (emphasizing local discontinuities). Some sequences of operations reduce some patterns to a set of blobs whose cardinality is significant. For each symbol and each sequence, the distribution of blob counts, if significant, is entered in a table which the computer may consult in its attempts to identify a symbol. It is hoped that such features as curvature and juxtaposition of singular features may eventually be recognized in this way, and further that the machine itself may hunt for the significant sequences for a given symbol by random trial, then rejection or judicious modification.

Douglas C. Engelbart

56-92

Programming Pattern Recognition—G. P. Dinneen. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 94–100; 1955.) This paper follows the article by O. G. Selfridge (56-91). Detailed description is given of the realization of the two operations (averaging and edging) on 90×90 spot-matrix patterns in the Memory Test Computer at Lincoln Laboratory. In order to try different sequences of operations on a given pattern it is necessary to provide room for three images: the original, the current working version, and a new one which may be under construction by some operation upon the working image. Averaging is accomplished by putting a dot in a given position of the new matrix if the number of dots within a 5×5 window surrounding the corresponding position in the working image is equal to or greater than a stated "threshold" number. There are sets of before-and-after photos showing the effects of different thresholds on different forms of block *A* letters. Edging maps zeros onto zeros, but may map a one (dot) onto either a one or a zero depending upon sort of a density-gradient check of the surrounding $n \times n$ window of the working-image spot. A count-weighting designation, the fraction of total ones-count in each window which will be the threshold number, and the value of n, all serve to specify a given edging operation. Photos show the effects of various edging operations on block *A's*, a square, and a block *O*. Blob isolation and counting are relatively easy, averaging takes 300 instructions and requires some twenty seconds per letter, while edging requires 700 registers of instructions and takes two minutes.

Douglas C. Engelbart

56-93

Generalization of Pattern Recognition in a Self-Organizing System—W. A. Clark and B. G. Farley. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 86–91; 1955.) This paper reports on a continuation of experiments on a system previously described in TRANS. IRE, vol. PGIT-4, pp. 76–84; September, 1954, by same authors. The Memory Test Computer at Lincoln Laboratory is programmed to simulate a sixteen-element model of a neutral-type net, with uniform-probability interconnections whose respective transmission weights are step-wise adjustable by a "modifier" unit. Weight is added to the contributing-input connections of just-fired elements upon favorable response, subtracted for unfavorable. Following is the authors' summary of this article: "Two further experiments to determine the system's properties have been carried out. The first demonstrates that self-organization still takes place even if the input patterns are subjected to considerable random variation. The second experiment indicates that, after organization with the usual fixed patterns, the system classifies other input patterns statistically according to a simple preponderance criterion. Significance of this result as a generalization in pattern recognition is discussed. Some remarks are made on methods of simulation of such systems and their relation to computer design."

Douglas C. Engelbart

BOOK REVIEWS

56-94

Tables of the Cumulative Binomial Probability Distribution—Staff of the Computation Laboratory. (*Annals Comput. Lab. Harvard Univ.*, vol. 35, Harvard Univ. Press, Cambridge, Mass., lxi+503 pp.; 1955.) This volume contains tables of the cumulative binomial probability distribution function

$$E(n, r, p) = \sum_{x=r}^{n} C_x^n p^x (1-p)^{x-n}$$

for $r=0(1)n$, $n=1(1)50(2)100(10)200(20)500(50)1000$, and for $p=0.01(0.01)0.50$ and $p=1/16,\ 1/12,\ 1/8,\ 1/6,\ 3/16,\ 5/16,\ 1/3,\ 5/8,\ 5/12$, and $7/16$. There are four parts to the introduction occupying some fifty pages of the book. The first part explains about binomial probability distributions, the second explains how the tables were prepared, the third explains recommended interpolation procedures, and the fourth has seventeen examples of applications of the tables. An appendix contains base ten logarithms of $n!$ for $n=0(1)1199$.

H. D. Huskey

56-95

Tables of the Function Arc Sin Z—Staff of the Computation Laboratory. (*Annals Comput. Lab. Harvard Univ.*, vol. 40, Harvard Univ. Press, Cambridge, Mass., xxxviii+586 pp.; 1956.) This volume gives values of arc sin z for portions of the first quadrant. Both the argument and the function are given in cartesian form. Various tables are given with increments in x and y ranging from 0.002 to 5. The first table with smallest increments covers an area in the vicinity of the branch point at $z=1$. Successive tables cover larger and larger areas up to maximum arguments of $x=475$, $y=350$, or $x=195$, $y=475$. Auxiliary tables for interpolation in the vicinity of the branch point are given in the introduction. In the body of the table, first and second order derivatives have been tabulated to assist in using second order interpolation formulas. The three parts of the introduction explain the arc sin function, the composition of the tables, and how to interpolate in the tables.

H. D. Huskey

56-96

Machine Translation of Languages (Fourteen essays)—edited by W. N. Locke and A. D. Booth. (Mass. Inst. of Tech., Cambridge, Mass.; John Wiley and Sons, N. Y.; Chapman and Hall, London, xii+243 pp.; 1955.) Large-scale computers can now perform exceedingly complex operations, mathematical and logical. They can be programmed to process vast amounts of data. Their "memories," in the form of punched cards or magnetic tapes, for example, can be tremendous. If languages consisted only of vocabulary and grammar, with one-to-one correspondences in meaning between the words of one language and those of another, and with the grammars of each formalizable as sets of logical rules, then an automatic dictionary would be a matter of input-output equipment, large enough memory capacity, and means for memory searching (all these exist in computers already), and machine translation would be possible when the automatic dictionary is augmented by a logical computer programmed to transform from one set of rules to another. The fourteen essays and historical introduction of this book trace the developments in and grapple with the problems of this field in its manifold aspects, engineering and linguistic. In a sense, some are concerned with bridging the gap between the problem of translation between natural languages and the aforementioned problem, the soluble one of translating between two completely formalized languages. The first essay (Weaver) is historically significant not only as the first presentation, apparently, of the general

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—*The Editor*

problem but also because of the leads for further research disclosed therein. The next (Richens and Booth) deals with some actual methods of mechanical translation, and specimens thereof, illustrating how problems such as stripping off endings to get at the root or how the wider problem of getting to the semantic units of the communication can be approached. The third essay (Oettinger) summarizes a thesis on the design of an automatic Russian-English technical dictionary. An experiment with monolingual volunteers showed with high probability that a scientist armed therewith could not only extract information clearly enough for his own purposes but could also communicate it to others. The next (Harper) goes into the syntax, morphology, and vocabulary of Russian, a specific mechanical translation procedure, and an example of its application. The eighth (Dostert) describes the Georgetown-I.B.M. experiment in which actual machine translation from Russian to English was done. The fifth essay (Bull, Africa, and Teichroew) goes in some detail into the problems of the "word," the interplay between dictionary and machine concepts of word, organization and size of machine memory and its connection with relative frequencies and other characteristics of language. The sixth essay (Locke) deals with the possibility of spoken, rather than written input, the seventh (Booth) with storage (memory) devices, and the ninth (Reifler) with the mechanical determination of meaning. The emphasis is on German, for which somewhat detailed analysis is given. Grounds are shown to exist for hoping that human preediting (to match text to machine capabilities) or postediting (to make the raw output more palatable linguistically) can be eliminated. A simplified English suited to the machine is exhibited next (Dodd). It is readily comprehended and sufficiently close to conventional English that a trained typist could simultaneously translate and type the input with little loss of speed. It may well be less expensive to take this approach initially than to handle the raw natural language with a machine capable of dispensing with preediting. Some practical development problems (Perry) of the general field are then treated; these are followed by a discussion of idioms (Bar-Hillel). The notion that idioms might foredoom mechanical translation to failure was dispelled for this reviewer, for an enlarged dictionary and more complicated searching are most of what idioms entail. Logical concepts of syntax (Wundheiler) and a discussion of syntax and the problem of multiple meaning (Yngve) close the book. The problem of technical translation alone is so pressing that development of mechanical methods is more than welcome. The book should be valuable not only as an excellent introduction to the field and a stimulus to further research; it may well help generate support for large-scale attack on the problem. It does not seem rash to assert that mechanical translation is not only possible but feasible and that it is fraught with profound implications for the future.

Jerome Rothstein
Courtesy of *Science*